datum inc
AUSTRON DIVISION

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# AUSTRON Model 2010B
# Disciplined Frequency Standard
Unit Serial No. _____

## Operation And Maintenance Manual
P/N 12794207, Revision C

June 19, 1995

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# INTRODUCTION

This manual is for personnel operating or maintaining the Model 2010B Disciplined Frequency Standard, Assembly P/N 25492147, manufactured by AUSTRON, Inc.

It contains information concerning the physical and electrical specifications, installation, adjustment and operational procedures, and theoretical descriptions. In addition, the manual provides assembly drawings, schematic and block diagrams.

## AMENDMENT NOTICE

AUSTRON, Inc. makes every attempt to provide up-to-date manuals with the associated equipment. Occasionally, changes are made to the equipment wherein it is necessary to provide amendments to the manual. If any amendments are provided for this manual they are printed on paper stock other than white and will be found at the rear of this manual.

### NOTE

The content of any amendments may effect operation, maintenance or calibration of the equipment.

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# 1. GENERAL DESCRIPTION

## 1.1. SCOPE OF SECTION

Section One introduces the AUSTRON Model 2010B Disciplined Frequency Standard. It is divided into two parts: a description of the purpose of the equipment and the physical and electrical specifications.

## 1.2. PURPOSE OF EQUIPMENT

The AUSTRON Model 2010B Disciplined Frequency Standard consists of an oscillator servo controlled locked system, and a high precision, electronic controlled oscillator module. The oscillator module is mounted within the chassis frame of the Model 2010B. The all digital memory control system and high stability rate generator lock the voltage-tuned frequency standard to the reference input. Manual slewing of the frequency standard aids rapid acquisition; decade slewing rate control is ganged to the CONTROL FREQUENCY display range switch for coarse, intermediate, and fine slewing. Panel meter and range switches indicate frequency control voltage. Range switch selects among four decades of sensitivity.

## 1.3. SPECIFICATIONS

The following table describes the physical and electrical specifications in the Model 2010B.

Table 1-1: Model 2010B Specifications

Physical Specifications

| | |
|---|---|
| Height | 3.5 in (8.9 cm) |
| Width | 17 in (43.1 cm) |
| Depth | 14 in (35.6 cm) |
| Weight | 20 lbs (9.1 kg) |
| Mounting | Rack or bench adapters supplied for standard 19-in (48.26 cm) rack mounting |

Electrical Specifications

| | |
|---|---|
| Power Input: | 115 Vac or 230 Vac ±15%, 48 Hz to 420 Hz, 20 A, or 22 Vdc through 32 Vdc |

SPECIFICATIONs (continued)

| | |
|---|---|
| **Reference Input:** | |
| Level | 1 to 10 Vp-p |
| Impedance | 680 Ω |
| Frequency | 1 MHz $\pm 10^{-7}$ |
| Connector | BNC, rear panel |
| **Standard Output:** | |
| Level | 5 Vp-p |
| Shape | 40 percent duty cycle |
| Rise/Fall Time | Less than 20 ns |
| Impedance | 50 Ω |
| Frequency | 1 MHz and 5 MHz (locked to the Reference Input) |
| Connectors | BNC, rear panel, two for each frequency |
| **Time Constants:** | |
| First Loop | 200,000 s |
| Second Loop | 50,000 s |
| Third Loop | 5 s, 230 s, or 5,000 s selected by front panel switch |
| **Temperature:** | 0°C to 50°C |

# 2. INSTALLATION

## 2.1. SCOPE OF SECTION

Section Two describes the steps required to prepare the Model 2010B Disciplined Frequency Standard for operation, or reshipment to another location. Steps include unpacking, inspection, installing and storing the unit, and a list of fundamental electrical requirements and accessories. Refer to Table 2-1 and Dwg. No. 12495413 for the rear panel controls, indicators and connectors for Model 2010B.

## 2.2. UNPACKING AND INSPECTION

As soon as the instrument is received, verify it is intact and as ordered. Inspect the unit for damage. If any shipping damage is found, refer to the warranty at the front of this manual and to paragraph 2.6 for repackaging and shipping instructions.

As soon as possible, install the instrument and give it a thorough electrical inspection. If the instrument fails to operate properly or to meet the listed specifications, immediately contact your AUSTRON representative.

## 2.3. EQUIPMENT SUPPLIED

The following accessories are supplied with the Model 2010B:

1. Three-wire 115 volts ac power cord.
2. Connector for standby dc power.
3. One Extender PCB.
4. Set of spare fuses and pilot lamps.
5. One alignment tool.

## 2.4. INITIAL INSTALLATION

The Model 2010B is mounted in any standard 19-inch (48.26 cm) rack with brackets provided or located on a bench. The unit operates on 25 watts of either 115 Vac or 230 Vac, 48 Hz to 420 Hz, single phase. However, before connecting the power cable to the source, verify that the voltage slide switch on the rear panel is in the appropriate position for the voltage to be used.

INITIAL INSTALLATION (continued)

To guard against line power failure, auxiliary dc power is connected at the rear panel connector labeled DC STBY. When a 22 Vdc through 32 Vdc source (capable of 0.8 A current) is connected, unit operation will be uninterrupted by line power failure. All functions of the equipment will operate normally from only the dc power source. Connections to the AN connector are as follows:

Pin A --- Battery positive
Pin B --- Battery negative (chassis ground)
Pin C --- No connection

Power up the Model 2010B at least two hours prior to normal operation to allow the 5 MHz crystal oscillator to stabilize. It is not necessary to connect any signal inputs or outputs during the initial warm-up period.

## 2.5. PRINTED CIRCUIT BOARDS

Exercise care when removing and reinstalling the printed circuit boards (PCBs) to ensure that connector contacts are not damaged. Recommended installation procedure is to slide the PCB carefully along the guide until resistance is met, then mate the contacts with a gentle, steady push.

## 2.6. STORAGE AND RESHIPMENT

To protect your instrument during shipment or storage, use the best packaging methods available. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1. Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2. If possible, use the original container designed for the instrument. Otherwise, use a strong carton 350 lb sq in bursting strength) or wooden box to house the instrument.

3. Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4. Seal the package with a strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

5. Refer to the warranty at the front of this manual and check with your AUSTRON representative for shipping instructions.

STORAGE AND RESHIPMENT (continued)

In all correspondence refer to the instrument by model number and full serial number.

## 2.7. REAR PANEL CONTROLS, INDICATORS AND CONNECTORS

The following table and diagram describe the rear panel controls, indicators and connectors for the Model 2010B.

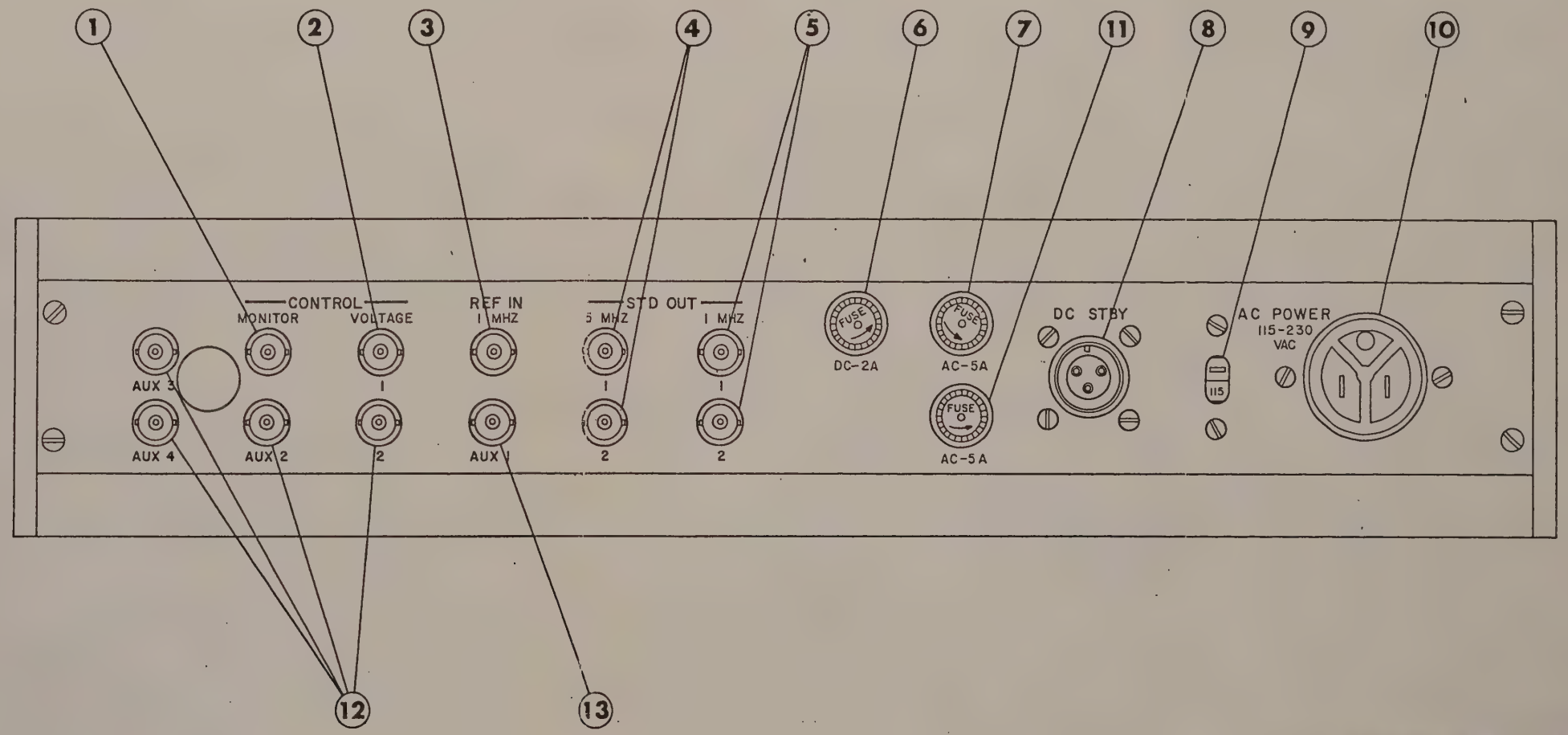
Table 2-1: Rear Panel Controls, Indicators and Connectors

| Reference | Name | Function |
|---|---|---|
| 1 | CONTROL MONITOR | Connector provides a dc voltage proportional to front panel meter reading, range is from 0 to 5 Vdc, 10 kΩ impedance |
| 2 | CONTROL VOLTAGE -1 | Connector provides a dc voltage proportional to oscillator control voltage, range is from 0 to 5 Vdc, 10 kΩ impedance |
| 3 | REF IN - 1 MHz | Connector provides input for 0.5 to 10 Vp-p, 1 MHz reference signal |
| 4 | STD OUT - 5 MHz | Connector provides 5 Vp-p square wave, 50 Ω impedance signal from 5 MHz crystal oscillator |
| 5 | STD OUT - 1 MHz | Connector provides 5 Vp-p, 40% duty cycle pulses, 50 Ω impedance signal from 5 MHz crystal oscillator |
| 6 | 5V REG-2A | 3AG-2 A fuse protects 5 volt power supply |
| 7 | AC-2A | 3AG-2 A fuse protects ac power |

REAR PANEL CONTROLS, INDICATORS AND CONNECTORS (cont'd)

| Reference | Name | Function |
|---|---|---|
| 8 | DC STBY | Connector provides input for dc standby power 22 Vdc to 32 Vdc at 0.5 A |
| 9 | 115/230 | Slide switch selects proper transformer connections for 115 Vac or 230 Vac operation |
| 10 | AC POWER | Connector provides input for ac power 115 Vac or 230 Vac ±15%, 48 Hz to 420 Hz |
| 11 | DC-5A | 3AG-5 A fuse protects dc power |
| 12 | AUX 2, 3, 4 and CONTROL VOLTAGE-2 | No connection |
| 13 | AUX 1 | Output for factory use during initial checkout |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | A | REDRAWN PER ECO 12060 MLN | 11/18/88 | GL |




FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO |
|---|---|---|---|
| | | | FIG. 3-2 |

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

| | | |
|---|---|---|
| Q.A. | Joe G | 18 Nov 88 |
| ENGR | CE | 17 Nov 88 |
| CHECKED | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

AUSTRON INC.
AUSTIN, TEXAS

REAR PANEL CONTROLS,
INDICATORS & CONNECTORS
MODEL 2010 B

| SIZE | C' | | |
|---|---|---|---|
| 3 | 2-5 | 12495413 | A |

SCALE

SHEET OF

# 3. OPERATING INSTRUCTIONS

## 3.1. SCOPE OF SECTION

Section Three provides instructions for the operation of the Model 2010B Disciplined Frequency Standard. It is divided into two major parts: function of controls, indicators and connectors; and step-by-step operating instructions.

## 3.2. FUNCTIONS OF CONTROLS, INDICATORS AND CONNECTORS

Dwg. No. 12495412 and Dwg. No. 12495413 show the controls, indicators and connectors on the front and rear panels of the Model 2010B RF Oscillator. Specific references and function descriptions are provided for front and rear panels in Tables 3-1 and 2-1.

Table 3-1: Front Panel Controls and Indicators

| Reference | Name | Function |
|---|---|---|
| 1 | ON | Toggle switch turns ac and dc power ON or OFF |
| 2 | LINE | Indicator lamp is ON when unit is operating on ac power |
| 3 | STBY | Indicator lamp is ON when unit is operating on dc power |
| 4 | CONTROL MODE | Rotary switch selects one of five operating modes |

CONTROL MODES

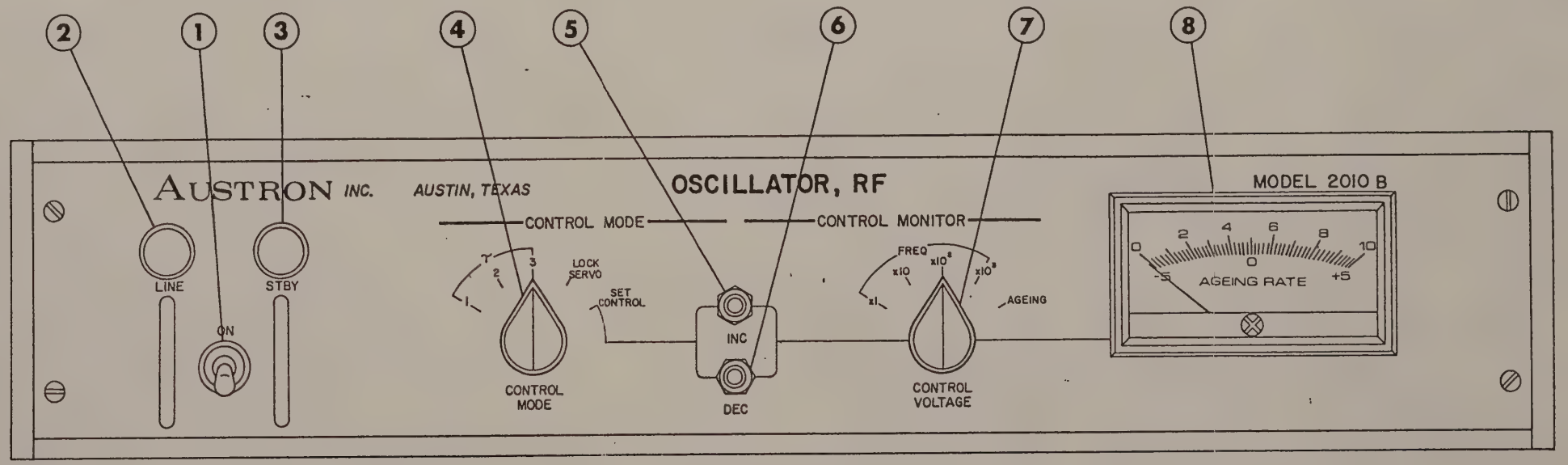
LOOP TIME CONSTANT (SEC)

| | First | Second | Third |
|---|---|---|---|
| $\tau 1$ | 5 | 50,000 | 200,000 |
| $\tau 2$ | 250 | 50,000 | 200,000 |
| $\tau 3$ | 5,000 | 50,000 | 200,000 |
| LOCK SERVO | Locked | Locked | Locked |

Front Panel Controls and Indicators (continued)

| Reference | Name | Function |
|---|---|---|
| | SET CONTROL | Locked * * |
| | | *Manually controlled by INC and DEC switches |
| 5 | INC | Push-button switch increases the dc voltage of the second or third loop as determined by the setting of the CONTROL VOLTAGE SWITCH when pressed and CONTROL MODE switch is in SET CONTROL position |
| 6 | DEC | Push-button switch decreases the dc voltage output of the second or third loop as determined by the setting of the CONTROL VOLTAGE SWITCH when pressed and the CONTROL MODE switch is in SET CONTROL position |
| 7 | CONTROL VOLTAGE SWITCH | Rotary switch selects meter range and determines the manual slewing rates |
| 8 | METER | Monitors oscillator control voltage and control loop outputs according to the setting of the front panel switches |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |

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|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | FIG. 3-1 |
| NEXT ASSY | USED ON | REF DES | FIG NO |

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED

| DECIMALS | FRACTIONS | ANGLES |
|---|---|---|
| | | |

MATERIAL:

| | | |
|---|---|---|
| QA | Joe Lee | 18 NOV 88 |
| ENGR | CE | 17 NOV 88 |
| CHECKED | CRL | 11-16-88 |
| DRAWN | MLN | 11-4-88 |

AUSTRON INC.
AUSTIN, TEXAS

FRONT PANEL CONTROLS & INDICATORS
MODEL 2010B

| SIZE | CC | | | |
|---|---|---|---|---|
| 3 | 3-3 | 12495412 | A | |

SCALE

SHEET OF

FUNCTIONS CONTROLS, INDICATORS AND CONNECTORS (cont'd)

3.2.1. Operate/Service Switch

The Operate/Service switch mounted within the Model 2010B chassis, as shown in Figure 3-2, decreases the time constants of the digital integrators. Under normal operating conditions, the switch is left in the OPERATE position. The SERVICE position of the switch is intended to speed the initial checkout of the unit. If during normal operation, the switch is accidentally placed in the SERVICE position, immediately return the switch to the OPERATE position and complete the following alignment steps.

Table 3-2: Alignment Procedure

1. Place the front panel CONTROL Mode switch in the SET CONTROL position.

2. Place the front panel CONTROL VOLTAGE switch in the FREQ X1 position.

*3. Press the INCREASE or DECREASE push button until the indicator on the front panel meter is positioned at center scale.

4. Place the CONTROL VOLTAGE switch in the AGING position.

5. Press the INCREASE or DECREASE push button until the meter indicator is positioned at center scale.

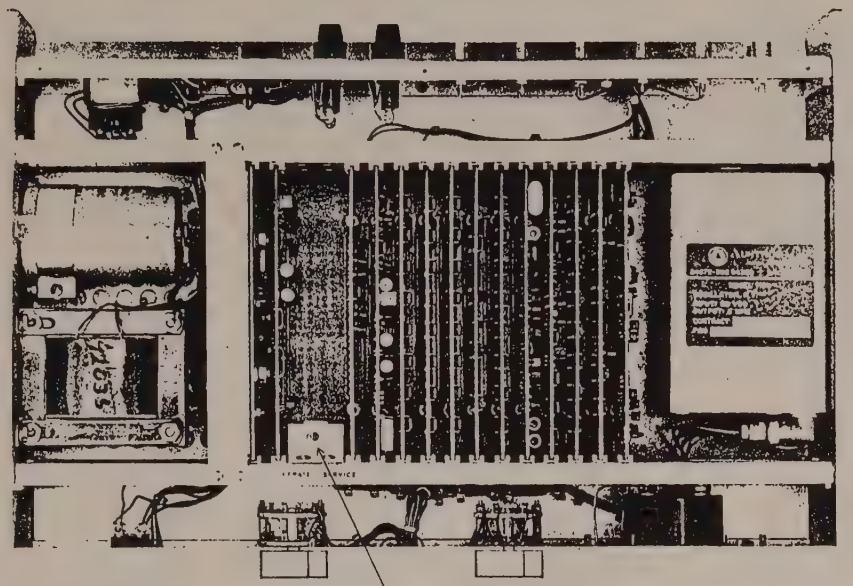
6. Return the CONTROL MODE switch to the T1 position.

*If the FREQ X 1, FREQ X 10, FREQ X $10^2$, FREQ X $10^3$, and AGING meter readings immediately prior to the time the OPERATE/SERVICE switch was accidentally placed in the SERVICE position are known, then the INCREASE and DECREASE push buttons can be used to return the unit to these readings.

FUNCTIONS OF CONTROLS, INDICATORS AND CONNECTORS
(continued)

The three servo loops reach their equilibrium states before the AGING reading on the meter stabilizes. It is necessary to wait about five days (several times the third loop time constant of 200,000 seconds) for the reading to stabilize. During this time, the 1 MHz and 5 MHz outputs is locked to the 1 MHz REF IN signal and may be used as if the loops had reached their equilibrium states. If the 1 MHz REF IN input is removed before the loops reach equilibrium, the 1 MHz and 5 MHz outputs take up the current frequency and aging rate set by the servo loops.

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | A | DRAWN PER ECO 12060 MLN | | |

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| | | | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | DEC | FRAC | ANG | | | | |
| | | | | MATERIAL: | | | CONTROLS, INTERNAL MODEL 2010 B | | | |
| | | | FIG.3-2 | Q.A. | | | SIZE 2 | CODE IDENT NO. 24672 | 12411826 | REV A |
| NEXT ASSY | USED ON | REF DES | FIG NO. | ENGR | | | | | | |
| APPLICATION | | | | CHECK | | | SCALE | | SHEET OF | |
| | | | | DRAWN | MLN | | | | | |

## 3.3. OPERATING INSTRUCTIONS OF MODEL 2010B

### 3.3.1. Basic Instructions.

The following are basic instructions for operating the Disciplined Frequency Standard. The instructions include steps for turning on the unit, setting servo loops, oscillator stabilization, and basic information on operating restrictions.

### 3.3.2. Model 2010B Power-up Procedure

After installing the Model 2010B according to Section Two, verify the power supply slide switch is in the appropriate position for voltage to be used. The following table describes the step-by-step procedure for power up.

Table 3-3: Model 2010B Power-up Procedure

| STEP | PROCEDURE |
|---|---|
| 1 | Verify power ac power setting (115 or 230 volts). |
| 2 | Set ON switch to ON. The LINE or STBY indicator lamp should come on. |
| 3 | Wait two hours after power-up for 5 MHz crystal oscillator to stabilize. |

### 3.3.3. Servo Loops Procedure

Following the two hour wait after power-up (paragraph 3.3.2), servo loops can be set.

Table 3-4: Servo Loops Procedure

1. Ensure the 1 MHz REFERENCE input is disconnected.
2. Trigger an oscilloscope from a 1 MHz frequency standard.
3. Connect the VERTICAL input of the oscilloscope to the 1 MHz STANDARD out.
4. Set the AGING meter indication to zero by utilizing the SET CONTROL position of the CONTROL Mode switch and the INCREASE and DECREASE push-button switches.

Servo Loops Procedure (continued)

5. Set the FREQUENCY X1 meter indication to midscale using the controls as in Step 4.

6. Set the CONTROL MODE switch to the LOCK SERVO position.

7. Observe the oscilloscope display. If the 1 MHz Standard output frequency waveform drifts less than 1 $\mu$s in a 100 s time period (frequency difference of less than $1o^{-8}$ between the trigger input and the 1 MHz STANDARD out), then no adjustment is necessary. If the drift is greater than 1 $\mu$s in 100 s, then adjust the trimmer capacitor in the Model 1150 oscillator (through the access hole in the rear panel) until the drift is within the above stated limit.

8. Go to OSCILLATOR STABILIZATION PROCEDURE.

---

Table 3-5: Oscillator Stabilization Procedure

---

| STEP | PROCEDURE |
|---|---|
| 1 | Set CONTROL Model to $\tau_1$ |
| 2 | Set CONTROL VOLTAGE to AGING |

NOTE

The three servo loops will have reached equilibrium when the METER reading stabilizes. Wait at least five days (two times as long as the third loop time constant of 200,000 s) for the reading to stabilize. During this time, the 1 MHz and 5 MHz outputs will be locked to the 1 MHz REF IN signal and may be used as if the loops had reached their equilibrium state. If the 1 MHz REF IN is removed before the loops reach equilibrium, the 1 MHz and 5 MHz OUTPUTS will take up the frequency and aging rate set by the servo loops.

Table 3-6: Post Oscillator Stabilization Procedure

| STEP | PROCEDURE |
|---|---|
| 1 | Set CONTROL VOLTAGE to desired position to monitor frequency or aging control voltage |
| 2 | Record METER readings at regular intervals |
| 3 | Set CONTROL MODE to $\tau_1$, $\tau_2$, or $\tau_3$, providing restrictions in paragraphs 3.3.5 and 3.3.6 are not exceeded |

NOTE

After a long interval of time, the X1 meter reading may approach full scale or zero. If so, repeat paragraph 3.3.3.

3.3.4. Open Loop Operation Procedure.

If a 1 MHz REF signal is not available, follow these steps.

Table 3-7: Open Loop Operation Procedure

| STEP | PROCEDURE |
|---|---|
| 1 | Set CONTROL MODE to SET CONTROL |
| 2 | Set CONTROL VOLTAGE to AGING |
| 3 | Press INC or DEC push-button switches until METER indicates zero aging rate at midscale |
| 4 | Set CONTROL VOLTAGE to X1, X10, X $10^2$ or X $10^3$ |
| 5 | Press INC or DEC push-button switches to change 5 or 1 MHz OUT frequency, set CONTROL MODE to LOCK SERVO |

OPERATING INSTRUCTIONS (continued)

NOTE

When in LOC SERVO position, the three loops are locked and will not respond to the INC or DEC switches or the 1 MHz REFERENCE INPUT. The 5 MHz crystal oscillator aging rate will be corrected by the rate locked in the third loop.

| STEP | PROCEDURE |
|---|---|
| 7 | After some time interval, measure output frequency and compute aging rate |
| 8 | Set CONTROL MODE to SET CONTROL |
| 9 | Set CONTROL VOLTAGE to AGING |
| 10 | Press INC or DEC switches to correct aging rate by computed amount. (See table below). |
| 11 | Set CONTROL VOLTAGE to X1, X10, $X10^2$ or $X\ 10^3$ |
| 12 | Press INC or DEC push-button switches to correct frequency by the computed amount. (See table below). |
| 13 | Readjust oscillator as required |

CONTROL VOLTAGE

| SWITCH POSITION | METER INDICATION, FULL SCALE |
|---|---|
| X1 | $1.4 \times 10^{-7}$ |
| X10 | $1.4 \times 10^{-8}$ |
| $X10^2$ | $1.4 \times 10^{-9}$ |
| $X10^3$ | $1.4 \times 10^{-10}$ |
| AGING | $-3 \times 10^{-9}$ |
| | $+3 \times 10^{-9}$/DAY |

OPERATING INSTRUCTIONS (continued)

3.3.5. Operating Restrictions

The 1 MHz REF IN signal cannot change phase more than about 0.5 $\mu$s during the time constant selected by the CONTROL MODE switch. If the phase change is larger, then the three loops will lose lock. If the unit loses lock, a shorter time constant must be selected or the 1 MHz REF IN phase change must be reduced.

3.3.6. 5 MHz Crystal Oscillator Aging Rate

The 5 MHz crystal oscillator aging rate cannot exceed $1.5 \times 10^{-9}$ or the third loop will lose lock.

# 4. FUNCTIONAL DESCRIPTION

## 4.1. SCOPE OF SECTION

Section Four details the theory of operation of the Model 2010B Disciplined Frequency Standard. Included are schematic and assembly drawings and a block diagram.

## 4.2. BLOCK DIAGRAM ANALYSIS

The Model 2010B is a high stability crystal oscillator controlled by an all-electronic third order servo loop. Dwg. No. 12494394 is a functional block diagram.

### 4.2.1. Crystal Oscillator

The 5 MHz output of the crystal oscillator is phase shifted and then buffered to produce the 5 MHz standard output. A divider (divide-by-5) and buffer amplifier produce the 1 MHz standard output. The A PHASE SHIFTER, controlled by the A PHASE DETECTOR, keeps the 5 and 1 MHz standard output signals phase-locked to the 1 MHz reference.

### 4.2.2. B and D Dividers

The outputs of B Divider and D Divider are phase detected and then filtered to produce the control voltage for the 5 MHz crystal oscillator. If the 5 MHz crystal oscillator frequency is not five times the 1 MHz reference frequency, the A PHASE SHIFTER appears between the output of B and D Dividers, changing the 5 MHz crystal oscillator control voltage. The control voltage is changed until the 5 MHz crystal oscillator frequency is five times the 1 MHz reference frequency.

### 4.2.3. D Phase Shifter

The outputs of B and C Dividers are compared and used to gate step commands to D PHASE SHIFTER. The step commands change the phase between the B and D Divider outputs, causing the control voltage to change. After the servo loops reach equilibrium, the step commands gated to D PHASE SHIFTER causes the control voltage to change at the rate necessary to correct for the 5 MHz crystal oscillator aging rate.

BLOCK DIAGRAM ANALYSIS (continued)

4.2.4. C Phase Shifter

The C PHASE SHIFTER is used to manually change the aging rate correction. The D PHASE SHIFTER is also used to manually change the control voltage.

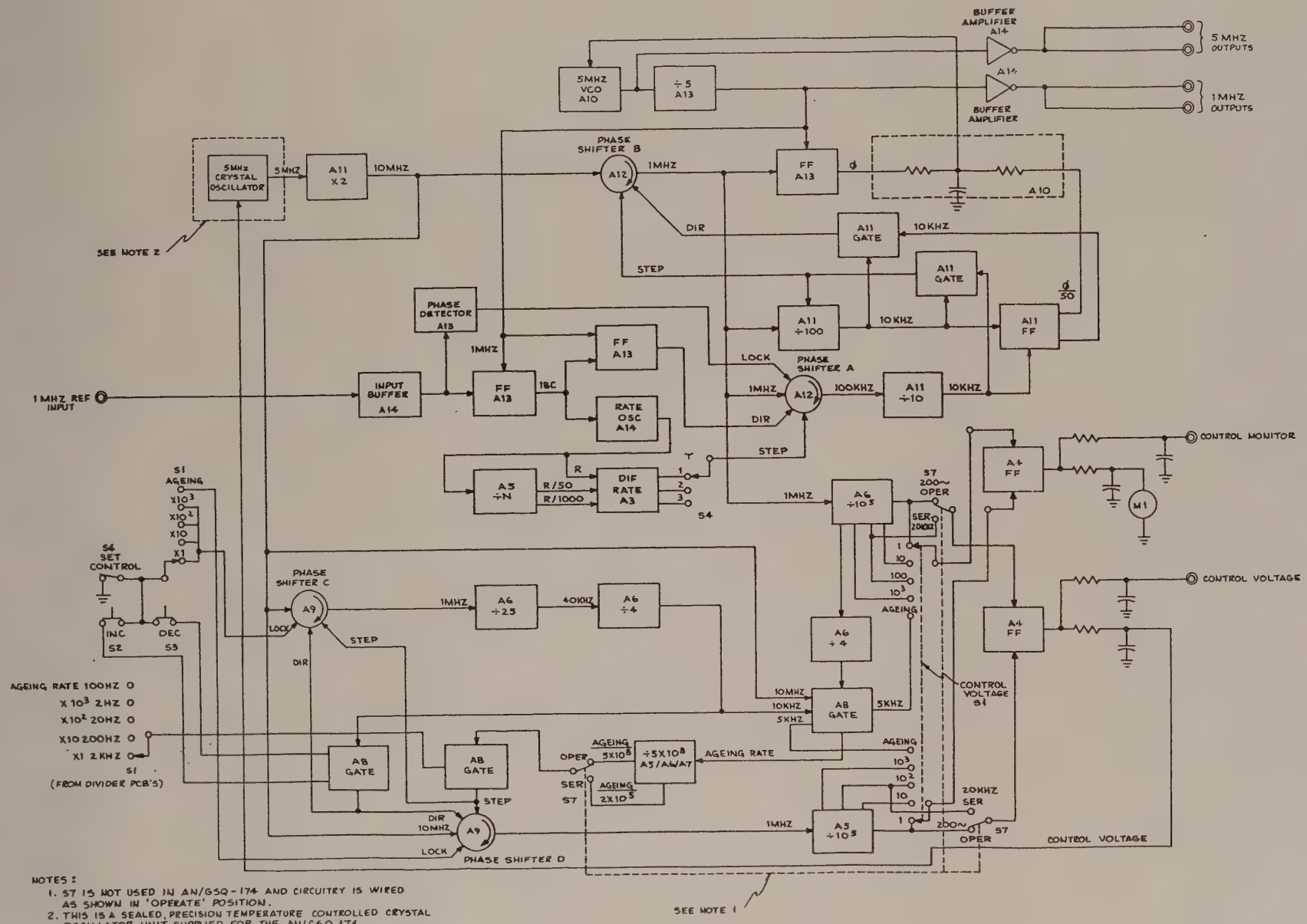
4.2.5. C Phase Detector

The C PHASE DETECTOR is switched between B, C and D Dividers to monitor the control voltage and aging rate correction.

4.3. CIRCUIT ANALYSIS

The following pages describe the Model 2010B circuitry in detail.

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




NOTES:
1. S7 IS NOT USED IN AN/GSQ-174 AND CIRCUITRY IS WIRED AS SHOWN IN 'OPERATE' POSITION.
2. THIS IS A SEALED, PRECISION TEMPERATURE CONTROLLED CRYSTAL OSCILLATOR UNIT SUPPLIED FOR THE AN/GSQ 174.

FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO. |
|---|---|---|---|
| APPLICATION | | | FIG. 4-7 |

TOLERANCES UNLESS OTHERWISE SPECIFIED

| DEC | FRAC | ANG |
|---|---|---|
| | | |

MATERIAL:

| | | |
|---|---|---|
| Q.A. | | 12 Nov 88 |
| ENGR | CE | 17 Nov 88 |
| CHECK | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

AUSTRON INC.
AUSTIN, TEXAS

BLOCK DIAGRAM
DISCIPLINED FREQUENCY STANDARD
MODEL 2010 B

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 2 | 2 4-3 2 | 12494394 | B |
| SCALE | | SHEET OF | |

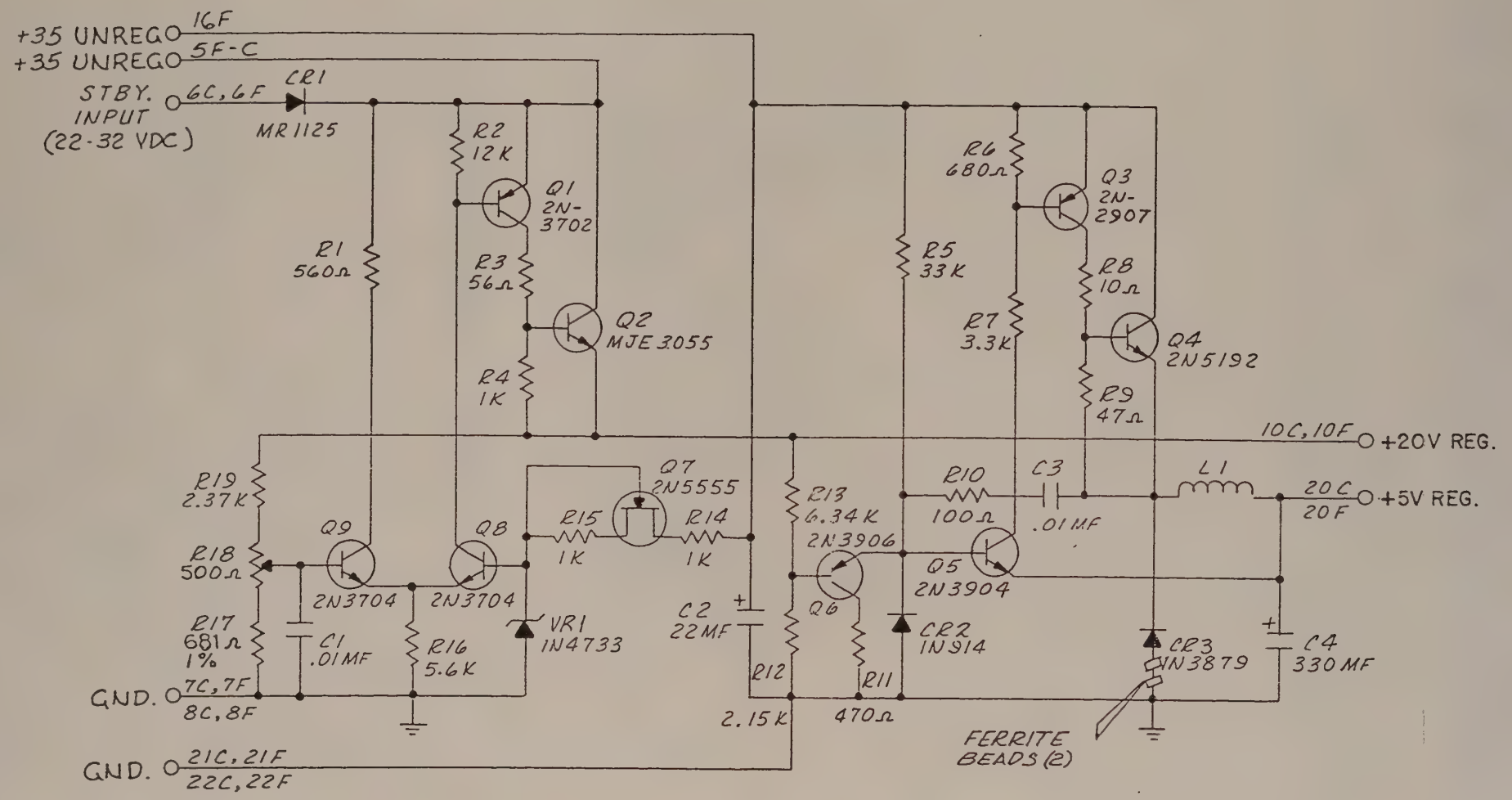
### 4.3.1. 20 Volt and 5 Volt Regulator PCB A1 (Schematic Dwg. No. 12392364)

The error (voltage difference) between the reference zener diode VR1 and variable resistor R18 is amplified by a differential amplifier, composed of transistors Q8 and Q9, then by transistor Q1. Q1 drives the series regulator transistor Q2. When the regulated output at pins 10F and 10C increases above 20 volts, the collector current of Q8 decreases, reducing the collector current of Q1 and decreasing the drive to Q2, thus decreasing the output to 20 volts. Transistor Q7 acts as a current source for VR1 and the base input of Q8, and provides isolation from the 35 Vdc unregulated supply.

Transistors Q3, Q4, Q5 and Q6 form a switching mode regulator. A 5 Vdc reference is derived from a voltage divider composed of R12 and R13. The emitter voltage of Q6 controls the nominal duty cycle of an oscillator formed by Q3, Q4 and Q5. When Q4 is conducting, the voltage at the input of the filter, consisting of inductor L1 and capacitor C4, is the unregulated supply voltage. When Q4 is not conducting, diode CR3 clamps the voltage at the input of the filter to ground. When the regulated output at pins 20C and 20F increases above 5 Vdc, Q5 stays on for a shorter length of time, which decreases the length of time Q3 and Q4 are turned on, thus shortening the positive duty cycle of the waveform at the emitter of Q4. As the average voltage at the input of the filter decreases, the output of the regulator returns to 5 Vdc.

N O T E S :

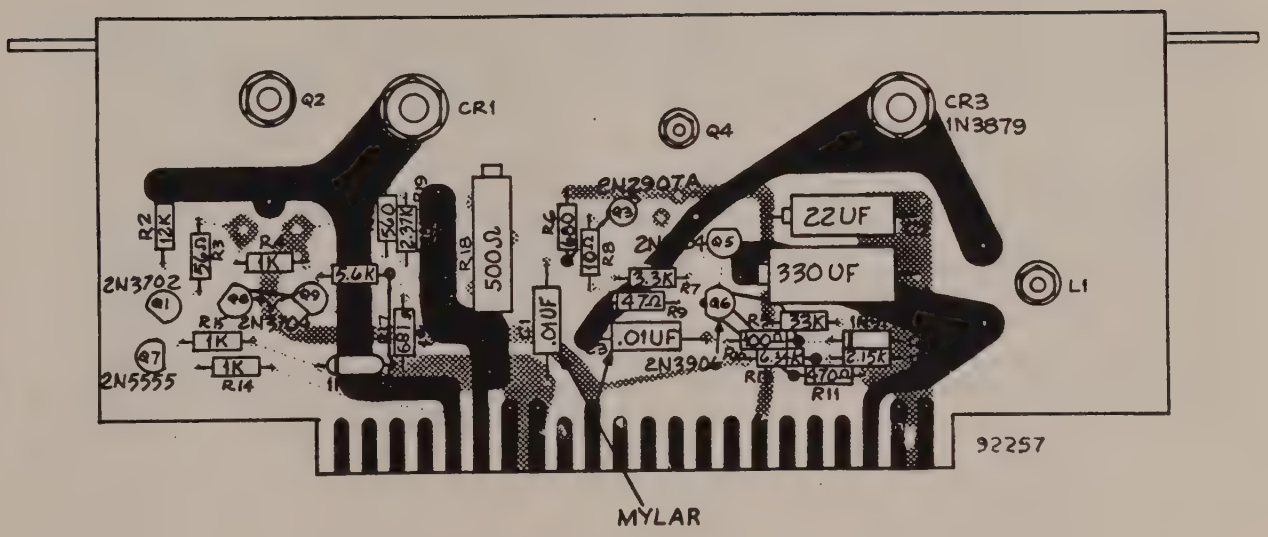
| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | D | R16 WAS 100Ω, R17 WAS 750Ω ECO. 2425 | 7-11-78 | |




FOR REFERENCE ONLY

| | | | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC AUSTIN, TEXAS | |
|---|---|---|---|---|---|---|---|---|
| | | | | DEC | FRAC | ANG | | |
| | | | | MATERIAL: | | | SCHEMATIC, +20V & +5V REGULATOR | |
| | 2010B | | | | | | SIZE 2 | COI NO 4-7 T 2 | 12392364 | D |
| NEXT ASSY | USED ON | REF DES | FIG NO | ENGR | | | | |
| APPLICATION | | | | CHECK | | | | |
| | | | | DRFTMN | LDP | 9-5-78 | SCALE | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| H | REDRAWN PER ECO 12060 MLN | | |




## ( COMPONENT SIDE )

FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | + 20 + 5 V REGULATOR MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | Joe | 12 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 10392258 REV H |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| APPLICATION | | CHECK | CRL | 11-16-88 | SCALE | | SHEET 1 OF 2 |
| | | DRAWN | MLN | 11-88 | | | |

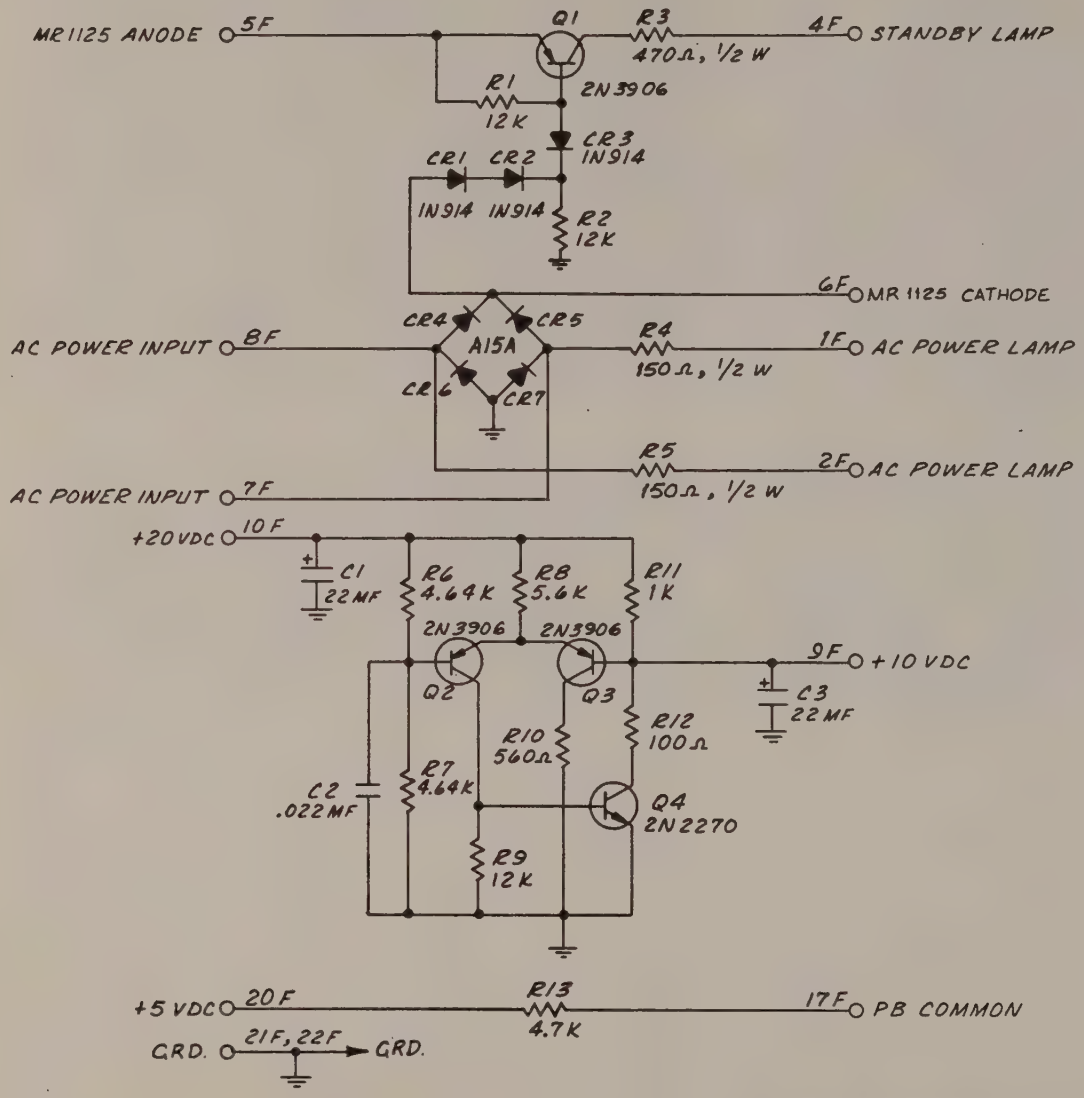
N O T E S :

### 4.3.2. 10 Volt Regulator PCB A2 (Schematic Dwg. No. 12392293)

The circuits on PCB A2 contain a line input rectifier, ac power lamp control, dc standby lamp control and 10 volts power supply regulator. Diodes CR4, CR5, CR6 and CR7 form a bridge rectifier which converts the ac line input to approximately 32 volts unregulated dc output at pin 6F. As long as the line input is present, current will flow through R5 to the ac power lamp. The positive dc standby input (nominally 24 volts) is connected to pin 5F. When the ac line input is present, the unregulated output at pin 6F will normally be more positive than the dc standby input, keeping the standby hold-off diode (CR1 on PCB A1) turned off and diodes CR1 and CR2 (on this board) turned on. The voltage drop across R2 keeps CR3 and Q1 turned off. In the absence of the ac line input, the unregulated voltage at the output of the bridge will drop until the standby hold-off diode on PCB A1 conducts. At the same time, the voltage across R2 will drop until CR3 conducts, turning on Q1 and lighting the standby lamp.

Transistors Q2, Q3 and Q4 form the 10 volt power supply regulator. Q2 and Q3 are a differential amplifier which compares the regulated 10 volt output at pin 9F to a 10 volt reference voltage derived from the regulated 20 volt input at pin 10F by a voltage divider formed by R6 and R7. Transistor Q4 is a parallel regulator. If the output at pin 9F goes positive with respect to the reference voltage, the voltage at the collector of Q2 will also go positive, causing Q4 to conduct harder and dropping the output voltage back to its normal level.

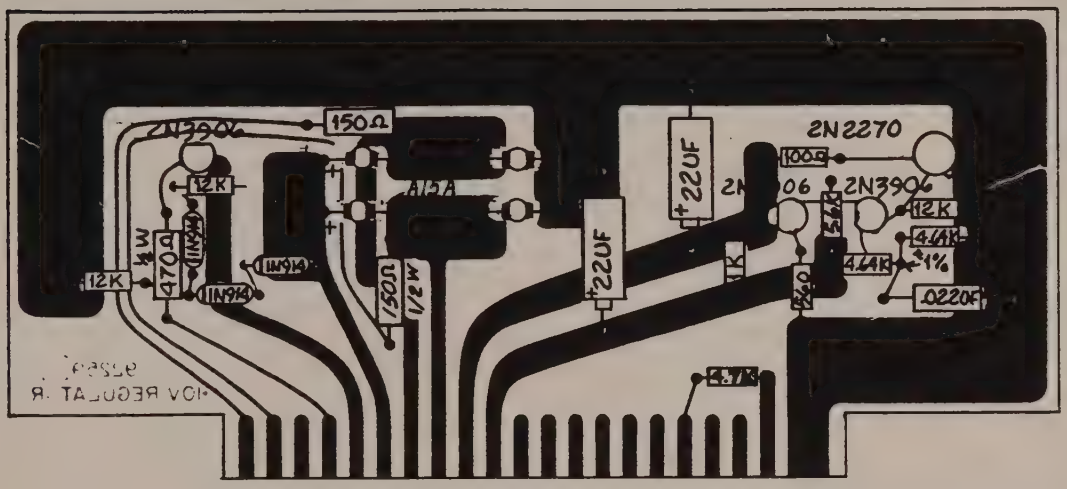
| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| C | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | + 10V REGULATOR MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| FIG. 6-2 | | Q.A. | | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 12392293 REV C |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11/16/88 | | | |
| APP | ION | DRAWN | MLN | 11-88 | SCALE | | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| D | REDRAWN PER ECO 12060 MLN | 11/18/88 | |




FOR REFERENCE ONLY

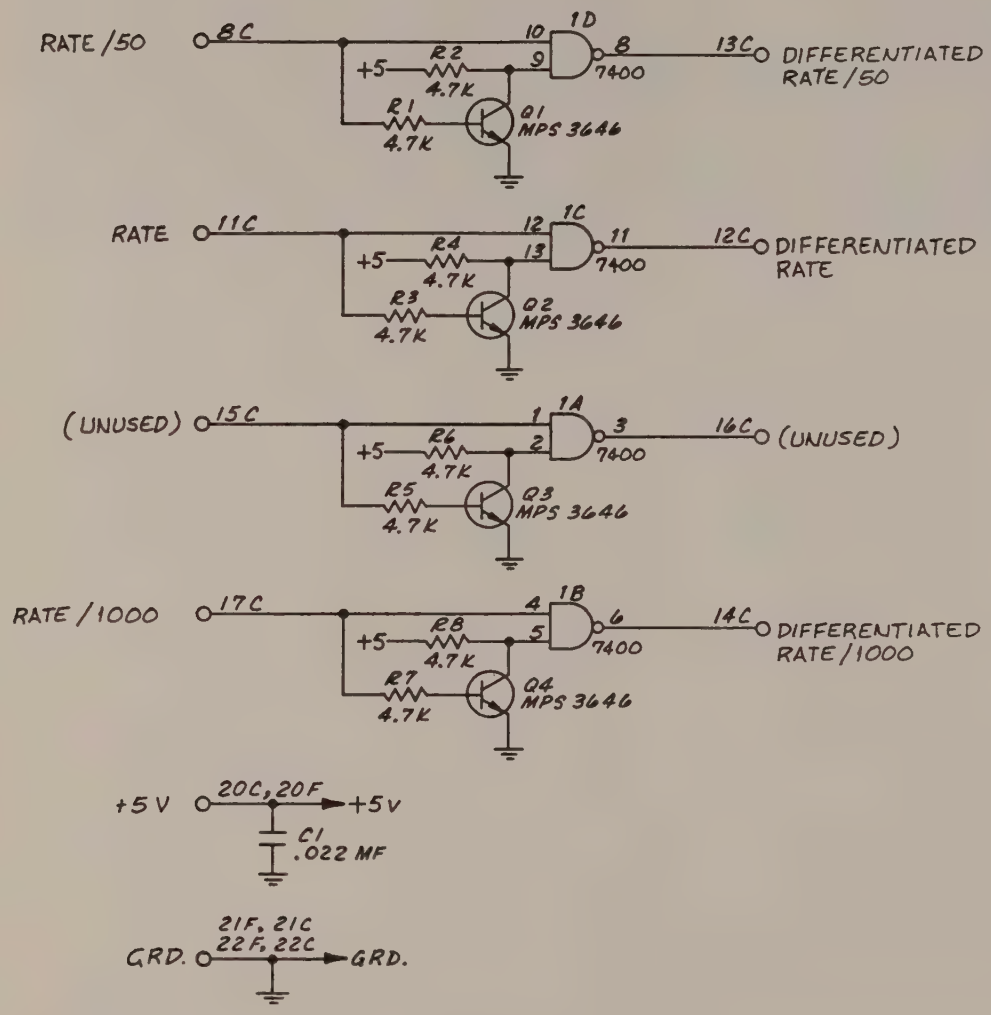
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | | |
| | | DEC | FRAC | ANG | | | | |
| | | MATERIAL: | | | +10V REGULATOR MODEL 2010B | | | |
| | | Q.A. | Joe | 11-16-88 | SIZE 1 | CODE IDENT NO. 24672 | 10392260 | REV D |
| NEXT ASSY | USED ON | ENGR | CF | 11-16-88 | | | | |
| APPLICATION | | CHECK | CRL | 11-16-88 | SCALE | | SHT | OF |
| | | DRAWN | MLN | 11-88 | | | | |

N O T E S :

### 4.3.3. Differentiator PCB A3 (Schematic Dwg. No. 12392287)

PCB A3 contains four transistor-integrated circuit differentiators. The circuit containing transistor Q1 and integrated circuit (U1D) is typical. Under normal conditions the input at pin 8C will be zero volts, which will keep Q1 turned off and provide inputs of 5 volts and zero volts at pins 9 and 10, respectively, of the integrated circuit. When the input at pin 8C goes positive, Q1 will turn on and (after a short length of time determined by the speed with which Q1 switches) the collector of Q1 will approach zero volts. During the period between the time the input at pin 8C goes positive and the time at which Q1 turns on, a narrow negative pulse with fast rise and fall times suitable for driving clock inputs on ICs is produced at pin 13C.

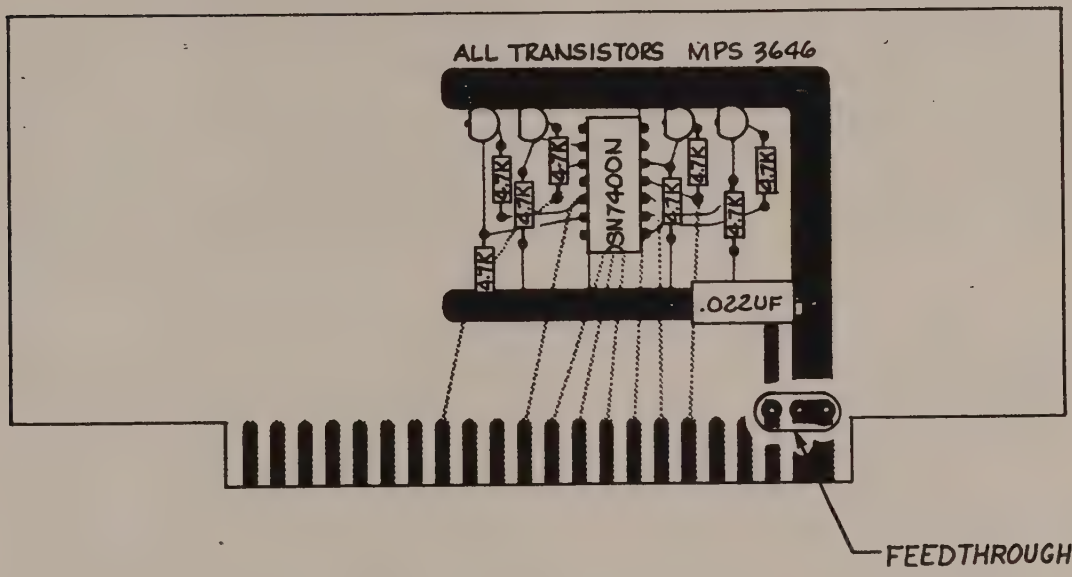
| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | | | |
| | | MATERIAL: | | | DIFFERENTIATOR BOARD MODEL 2010B | | |
| | FIG. 6-3 | Q.A. | Joe L | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 12392287 REV A |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLI | N | DRAWN | MLN | 11-88 | SCALE | | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | DIFFERENTIATOR MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | Joe K | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 10392248 REV B |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLICATION | | DRAWN | MLN | 11-88 | SCALE | | OF |

N O T E S :

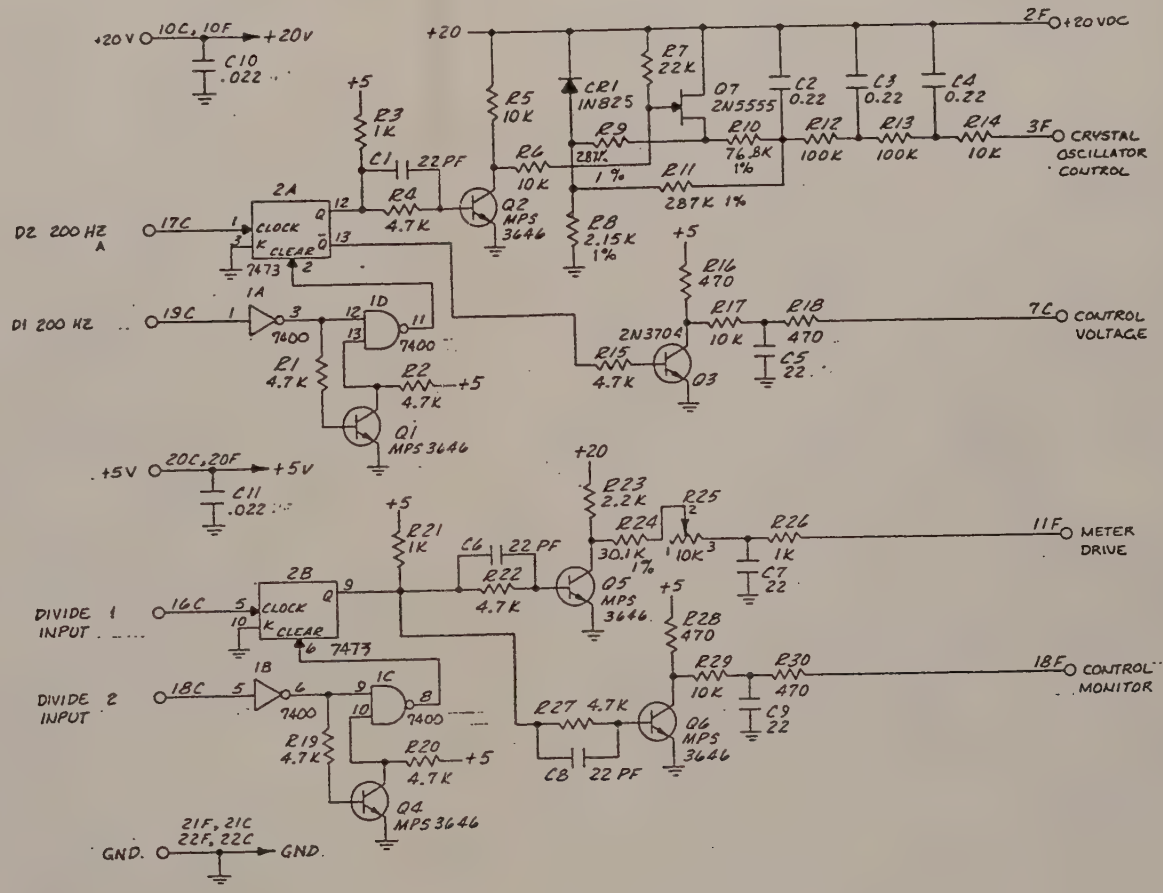
### 4.3.4. Phase Comparator PCB A4 (Schematic Dwg. No. 12392284)

The square wave input at pin 19C is inverted by IC (1A) and differentiated by transistor Q1 and IC (U1D) before being applied to the clear input of a J-K flip-flop IC (U2A). The outputs of the flip-flop at pins 12 and 13 are two complementary, variable duty cycle square waves. The duty cycles of the square waves are proportional to the relative phase difference between the inputs at pins 17C and 19C. The $\bar{Q}$ output is inverted by transistor Q3 and filtered by resistor R17 and capacitor C5 to produce a dc output at pin 7C suitable for driving an external recorder. Pin 7C is connected to the CONTROL VOLTAGE jack on the rear panel. The Q output of IC (U2A) is inverted by transistor Q3 and used to drive the gate input of field effect switch Q7. Transistor Q7, zener diode VR1, and resistor R8, R9, R10 and R11 form a precision switching network which, in conjunction with a low-pass filter (C2, C3, C4, R12, R12 and R14), provides the control voltage input for the crystal oscillator.

Transistor Q4 and ICs (U1B), (U1C), and (U2B) form a phase comparator similar to the one described above. The Q output of IC (U2B) is inverted by transistor Q5 and filtered by resistor R24 and capacitor C7 to produce a dc output at pin 11F which is used to drive the front panel meter. R25 limits the current at the output and is used to calibrate the meter. The Q output of IC (U2B) is also inverted by transistor Q6 and filtered by resistor R29 and capacitor C9 to produce a dc output at pin 18F suitable for driving an external recorder. Pin 18F is connected to the CONTROL MONITOR jack on the rear panel.

N O T E S :

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | B | ECO 946 | 4/8/75 | WWK |
| | C | REDRAW WITH CORRECTIONS PER ECO 7438 | | |




FOR REFERENCE ONLY

2. CAPACITOR VALUES IN MICROFARADS.
1. RESISTOR VALUES IN OHMS.
NOTES: UNLESS OTHERWISE SPECIFIED

| | | | |
|---|---|---|---|
| 10392213 | 2010B | A4 | |
| NEXT ASSY | USED ON | REF DES | FIG NO |
| APPLICATION | | | |

TOLERANCES UNLESS OTHERWISE SPECIFIED

| DECIMALS | FRACTIONS | ANGLES |
|---|---|---|
| | | |

MATERIAL:

ENGR
CHECKED
DRAWN 5/31/ac

AUSTRON INC.
AUSTIN, TEXAS

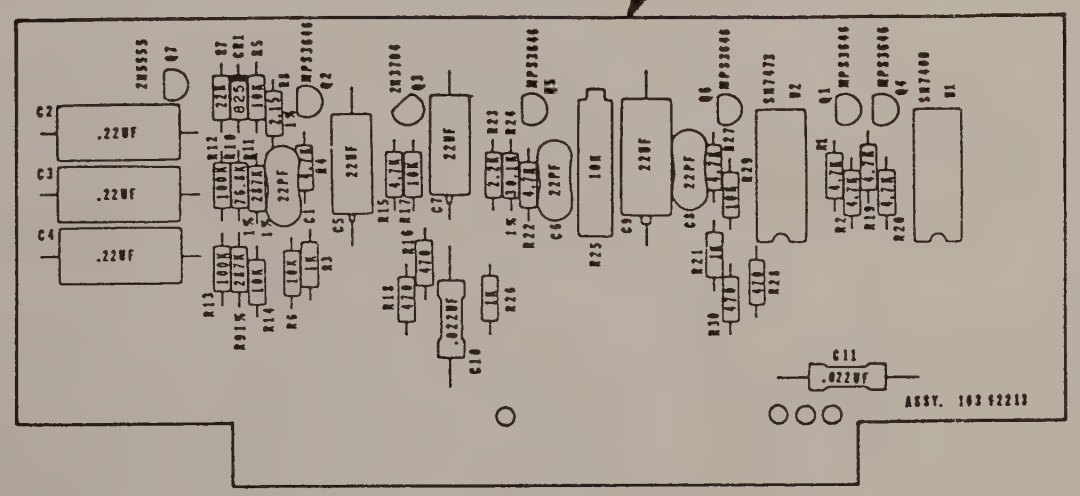
SCHEMATIC-
PHASE COMPARATOR

SIZE 3 | CODE IDENT NO. 4-21 2 | 12392284

SCALE NONE | SHEET 1 OF

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | C | REDRAW W/CORRECTIONS; ECO 7438 | 6-4-85 | OK |
| | D | P/C REVISED PER ECO 10627 D7 | 2-10-87 | CRL |

00392212




FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO. |
|---|---|---|---|
| | 2010B | | |

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED

| DEC | FRAC | ANG |
|---|---|---|
| | | |

MATERIAL:

| | | |
|---|---|---|
| Q.A. | | |
| ENGR | | |
| CHECK | [illegible] | 6-11-85 |
| DRAWN | John Mack | 6/7/85 |

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY-
PHASE COMPARATOR

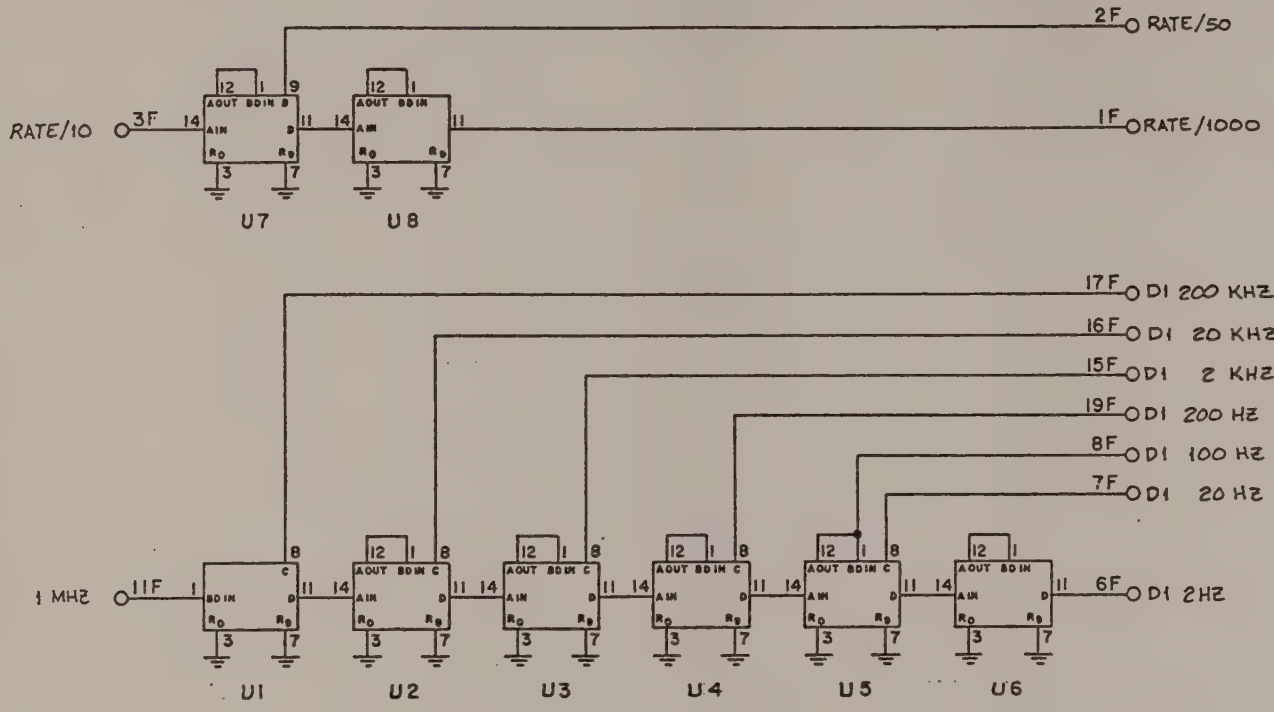
| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 2 | 14-23 | 10392213 | D |

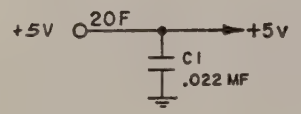
SCALE 1:1 SHEET 1 OF 1

### 4.3.5. Divider 1 PCB A5
(Schematic Dwg. No. 12392292)

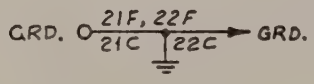
PCB A5 contains eight SN7490N IC dividers arranged in two separate sections. ICs (U1) through (U6) are arranged in series to provide a total division ratio of 500,000. IC (U1) is connected as an N/5 divider. ICs (U2) through (U6) are connected as N/10 dividers. Intermediate division rates are brought out on pins 17F, 16F, 15F, 19F, 8F and 7F. ICs (U7) and (U8) are connected in series to provide an N/5 output at 2F and an N/100 output at pin 1F.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




U1 THRU U8-SN7490N




FOR REFERENCE ONLY

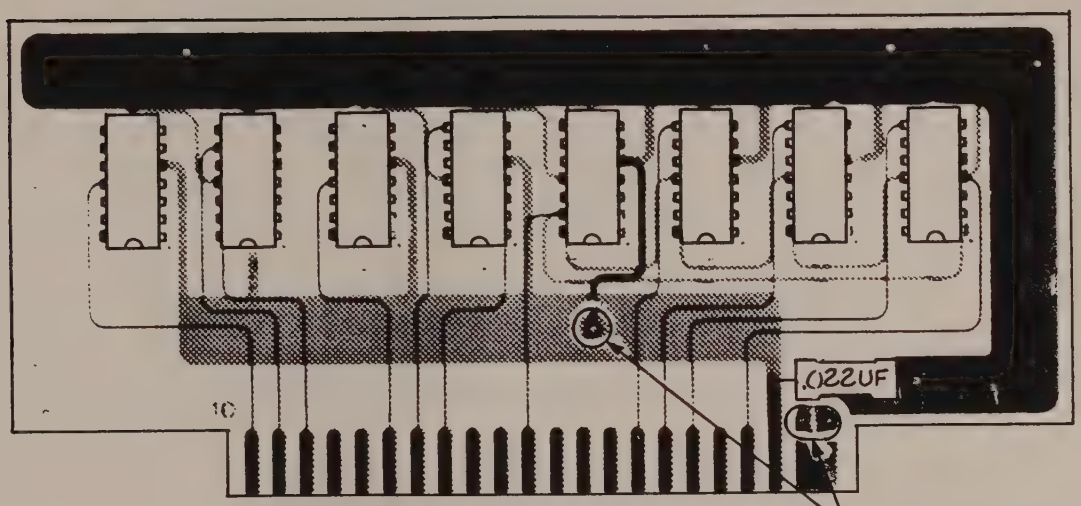
| TOLERANCES UNLESS OTHERWISE SPECIFIED | | |
|---|---|---|
| DEC | FRAC | ANG |
| MATERIAL: | | |

AUSTRON INC.
AUSTIN, TEXAS

**DIVIDER 1 BOARD**
**MODEL 2010B**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FIG. 6-5 | Q.A. | | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 12392292 | REV A |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLI 4-26 | N | DRAWN | MLN | 11-88 | SCALE | | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




ALL IC'S ARE SN7490N.

FEEDTHROUGH HOLES

FOR REFERENCE ONLY

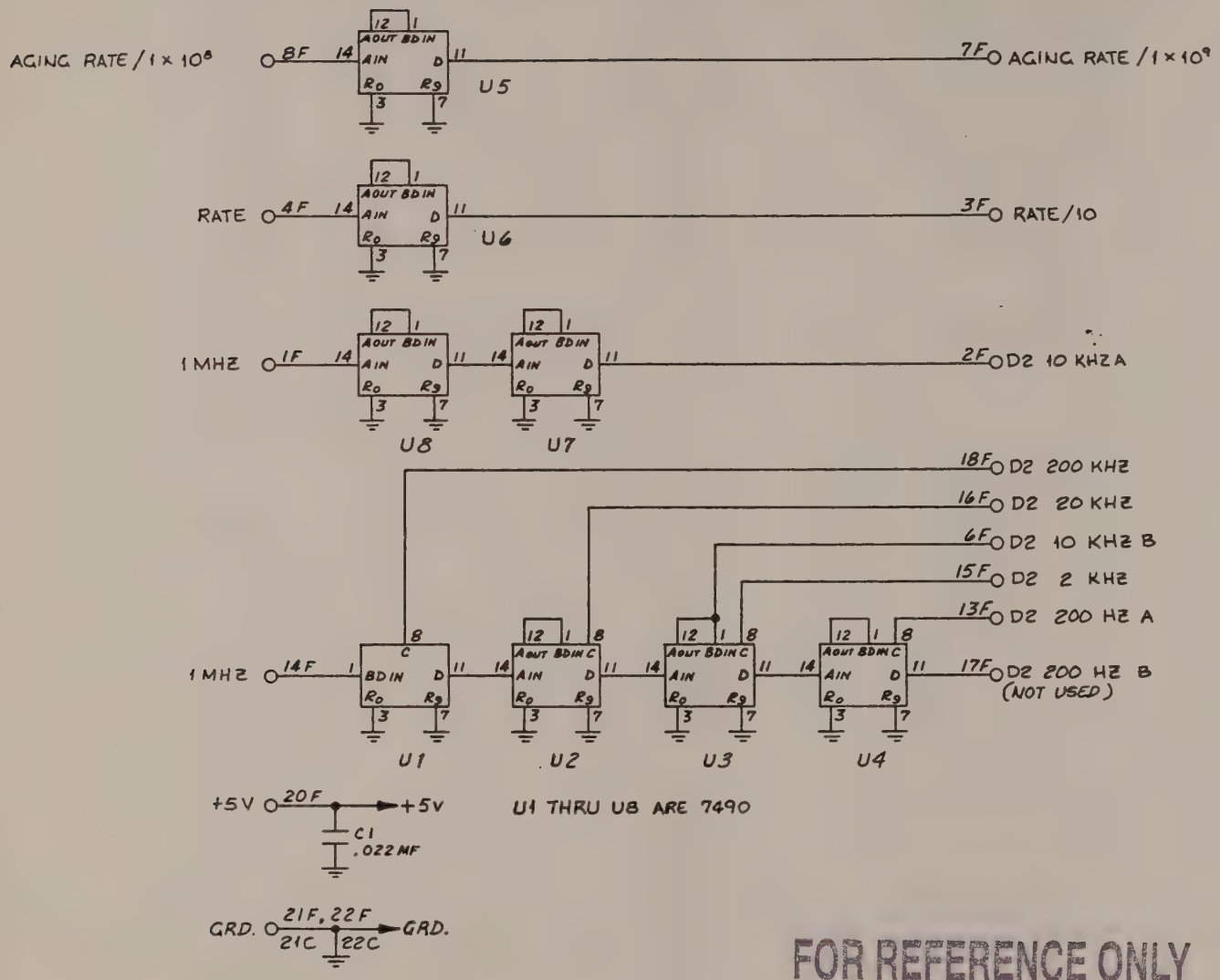
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | DIVIDER 1 BOARD MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | Joe K | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 10394383 REV B |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLICATION | | DRAWN | MLN | 11-88 | SCALE | | OF |

N O T E S :

4.3.6. Divider 2 PCB A6
(Schematic Dwg. No. 12392291)

PCB A6 contains eight SN7490N IC dividers arranged in four separate sections. ICs (U1) through (U4) are arranged to provide a total division ratio of 5,000. Intermediate division ratio signals are brought out on pins 18F, 16F, 6F, 15F and 13F. IC (U5) divides the input at pin 8F by ten. IC (U6) divides the input at pin 4F by ten. ICs (U7) and (U8) are connected to divide the input pin 1F by 100.

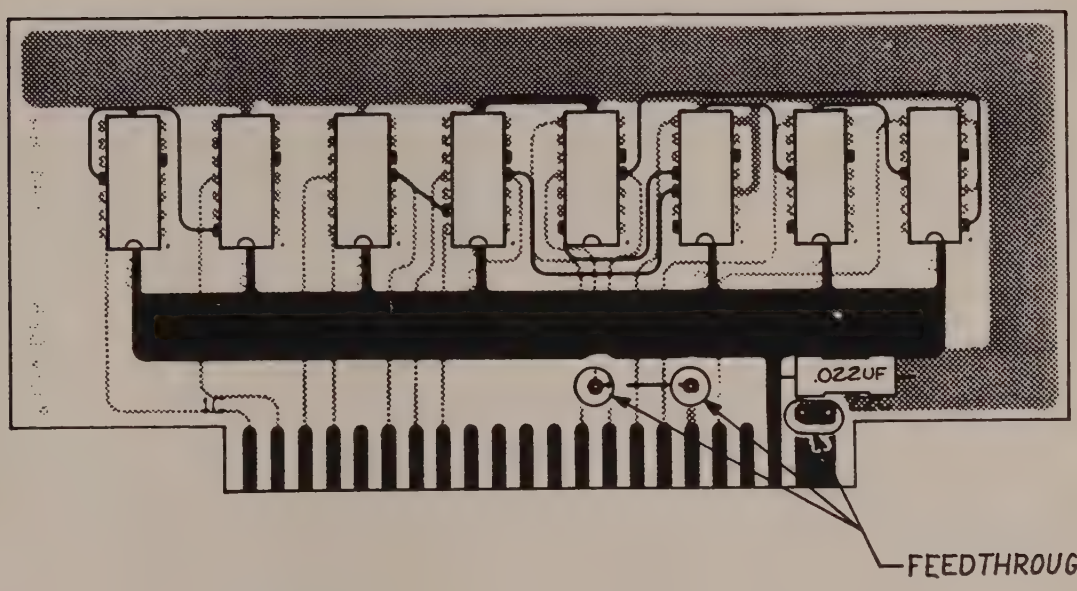
| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | | | |
| | | MATERIAL: | | | DIVIDER 2 BOARD MODEL 2010B | | |
| | FIG. 6-6 | Q.A. | Joe Lee | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 12392291 REV A |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPI | ON | DRAWN | MLN | 11-88 | SCALE | | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| C | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




NOTES:

1. ALL IC'S ARE SN7490N.

FOR REFERENCE ONLY

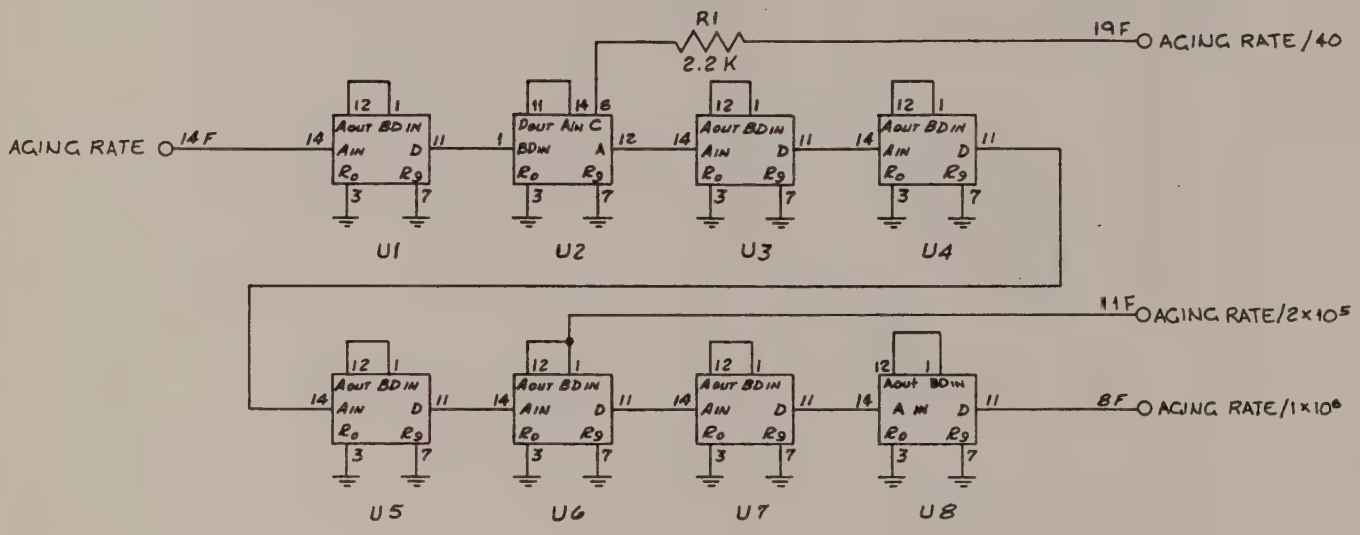
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | DIVIDER 2 BOARD MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | Joe Le | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 10394385 REV C |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLICATION | | DRAWN | MLN | 11-88 | SCALE | | ET OF |

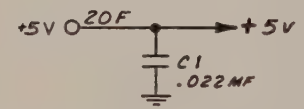
N O T E S :

4.3.7. Divider 3 PCB A7
(Schematic Dwg. No. 12392290)

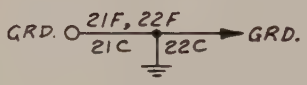
Eight SN7490N ICs are connected in series to divide the input frequency at pin 14F by 100,000,000. The eight SN7490Ns are connected at N/10 dividers.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |



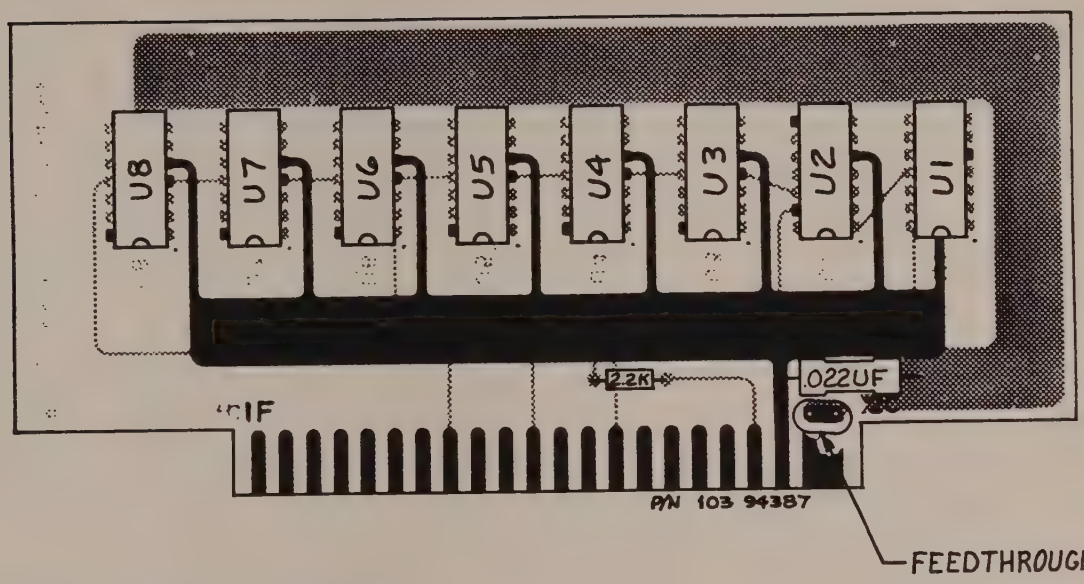

U1 THRU U8 ARE 7490




FOR REFERENCE ONLY

| | | | | | | |
|---|---|---|---|---|---|---|
| TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | | |
| DEC | FRAC | ANG | | | | |
| MATERIAL: | | | DIVIDER 3 BOARD MODEL 2010B | | | |
| FIG. 6-7 | Q.A. | Joe Le | 18 Nov 88 | SIZE 1 | CODE IDENT NO. 24672 | 12392290 REV A |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | |
| | | CHECK | CRL | 11-16-88 | | |
| APPLIC | | DRAWN | MLN | 11-88 | SCALE | SHEET OF |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO12060 MLN | 11/18/88 | CRL |




NOTES:

1. ALL IC'S ARE SN7490.

FOR REFERENCE ONLY

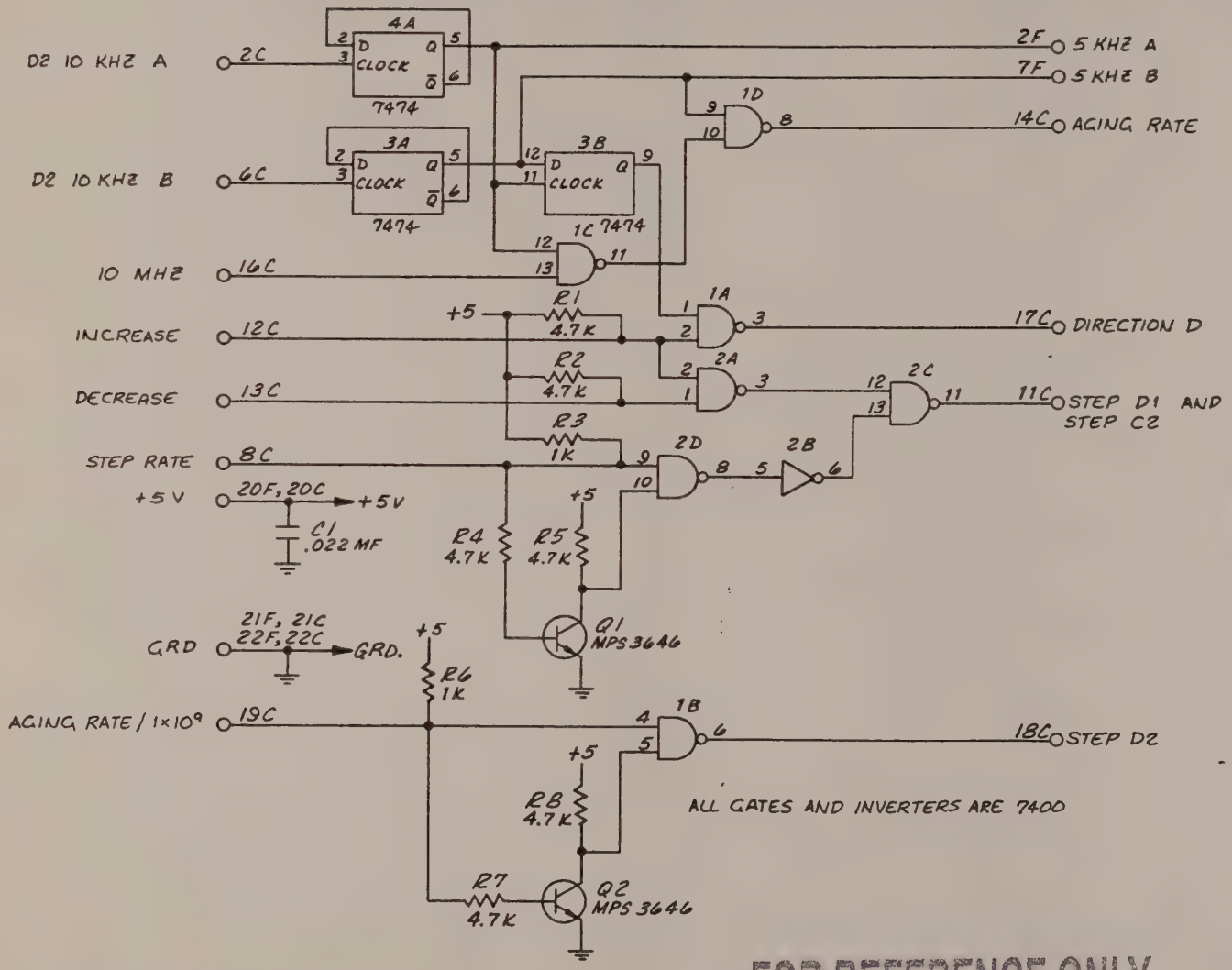
| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | | |
| | | DEC | FRAC | ANG | | | | |
| | | MATERIAL: | | | DIVIDER 3 BOARD MODEL 2010B | | | |
| | | Q.A. | | 18 Nov 88 | SIZE | CODE IDENT NO. | | REV |
| | | ENGR | CE | 17 Nov 88 | 1 | 24672 | 10394387 | A |
| NEXT ASSY | USED ON | CHECK | CRL | 11/16/88 | | | | |
| APPLICATION | | DRAWN | MLN | 11-88 | SCALE | | | OF |

N O T E S :

### 4.3.8. Servo Control PCB A8
### (Schematic Dwg. No. 12392288)

A differentiating circuit, formed by transistor Q2 and IC (U1B), produces narrow negative-going pulses at the trailing edges of the square wave input at pin 19C. The output of the differentiator is connected to the step input of one section of a dual phase shifter, A9. The 10 MHz signal present at pin 16C is gated with 5 kHz signals (derived from the 10 kHz inputs at pins 2C and 6C) to produce the aging correction output at pin 14C. The 5 MHz signals are also brought out on pin 2F and 7F.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/16/88 | CRL |




FOR REFERENCE ONLY

| TOLERANCES UNLESS OTHERWISE SPECIFIED | | |
|---|---|---|
| DEC | FRAC | ANG |
| MATERIAL: | | |

AUSTRON INC.
AUSTIN, TEXAS

**SERVO CONTROL BOARD**
**MODEL 2010B**

FIG. 6-8

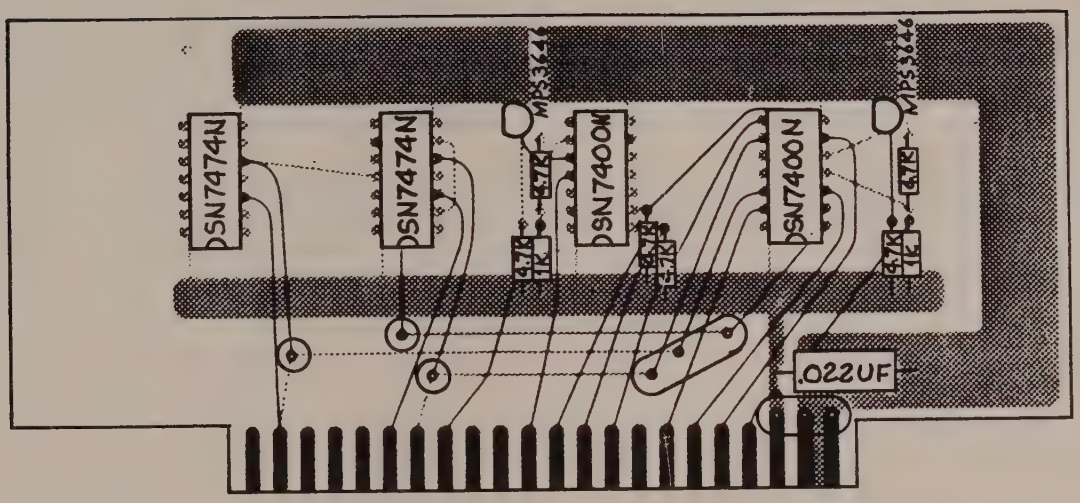
| | | |
|---|---|---|
| Q.A. | Joe K | 18 NOV 88 |
| ENGR | CE | 17 Nov 88 |
| CHECK | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 1 | 24672 | 12392288 | A |
| SCALE | | SHEET OF | |

NEXT ASSY | USED ON

APPLIC

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




NOTES:

1. CIRCLED HOLES ARE FEEDTHROUGH HOLES

FOR REFERENCE ONLY

| NEXT ASSY | USED ON |
|---|---|
| APPLICATION | |

TOLERANCES
UNLESS OTHERWISE SPECIFIED

| DEC | FRAC | ANG |
|---|---|---|
| | | |

MATERIAL:

| | | |
|---|---|---|
| Q.A. | Joe L | 8 NOV 88 |
| ENGR | CE | 7 NOV 88 |
| CHECK | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

AUSTRON INC.
AUSTIN, TEXAS

SERVO CONTROL
MODEL 2010B

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 1 | 24672 | 10392216 | B |
| SCALE | | | OF |

N O T E S :

### 4.3.9. Dual Phase Shifter PCBs A9 and A12 (Schematic Dwg. Nos. 12392282-01 and 12392282-02)

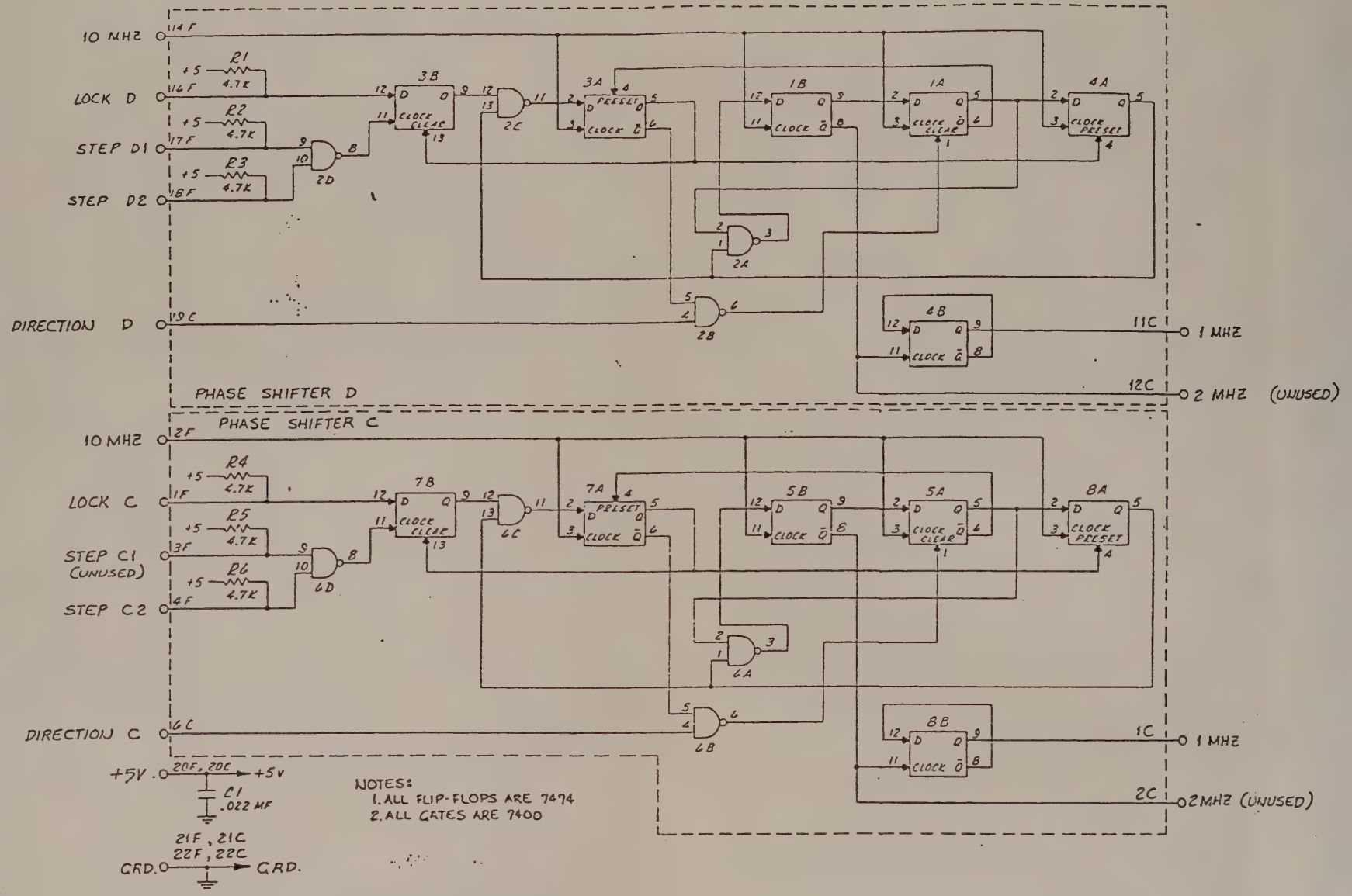
The circuits on PCBs A9 and A12 each contain two separate variable ratio dividers. Each divider normally divides the clock input (pins 14F and 2F) by five. N/5 outputs are provided at pins 12C and 2C. N/10 outputs are provided at pins 11C and 1C. A direction input is provided (pins 19C and 6C) to control the abnormal division ratio (either N/4 or N/6) and step inputs are provided (pins 17F, 18F, 3F and 4F) to control when abnormal division will occur.

For example, if a negative-going step input occurs while the direction input is a logical ONE (5 volts), the output of the variable ratio divider will retard by one cycle of the input frequency. If a negative-going step input occurs while the direction input is a logical ZERO (zero volts), the output of the variable ratio divider will advance by one cycle of the input frequency. If no step inputs occur, the divider will produce an output at one-fifth of the input frequency, regardless of the value of the direction input.

A lock input (pins 16F and 1F) is also supplied. If the lock input is a logical ZERO, then the step commands will have no effect on the divider.

N O T E S :

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | | | | |




FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO |
|---|---|---|---|
| | 2010B | A9 | |

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

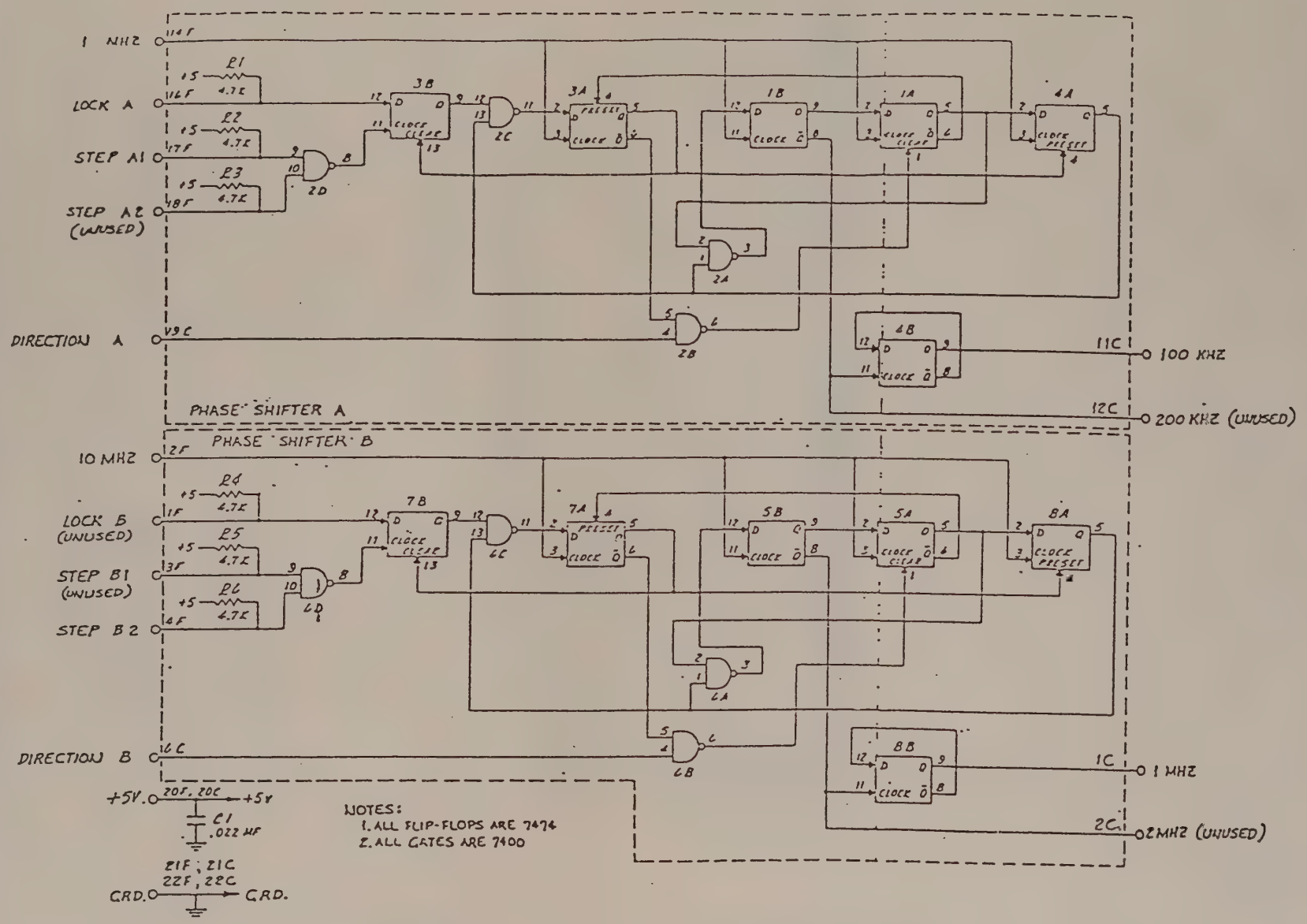
ENGR
CHECKED

AUSTRON INC.
AUSTIN, TEXAS

SCHEM,
DUAL PHASE SHIFTER
MODEL 2010B - A9

SIZE 3 | 4-43 | 12392282-1 | —

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | | | | |




FOR REFERENCE ONLY

| | | | | |
|---|---|---|---|---|
| | 2010B | A12 | | |
| NEXT ASSY | USED ON | REF DES | FIG NO | |

APPLICATION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

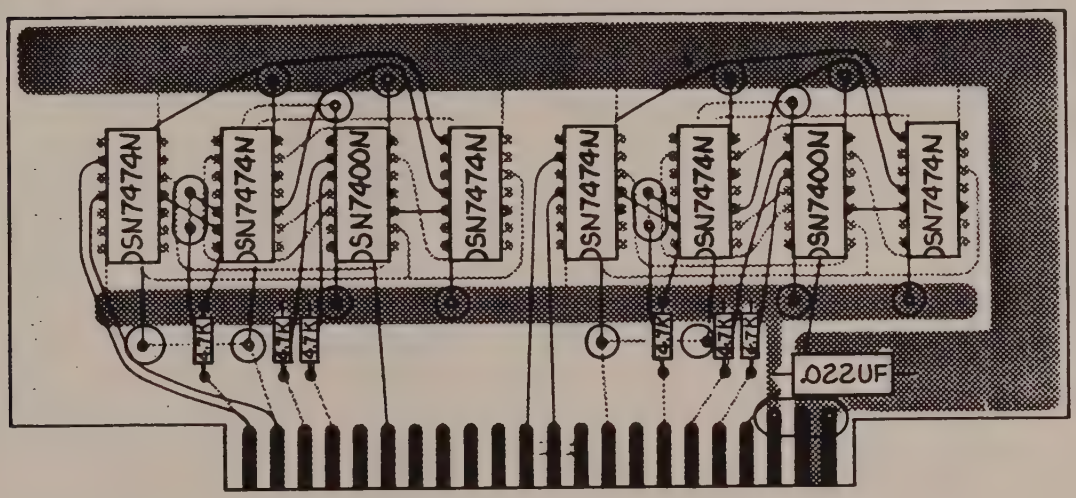
ENGR
CHECKED

AUSTRON INC
AUSTIN, TEXAS

SCHEM,
DUAL PHASE SHIFTER
MODEL 2010B - A12

SIZE 3 | 4-45 | 12392282-2 | —

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




NOTES:
1. CIRCLED HOLES ARE FEEDTHROUGH HOLES

FOR REFERENCE ONLY

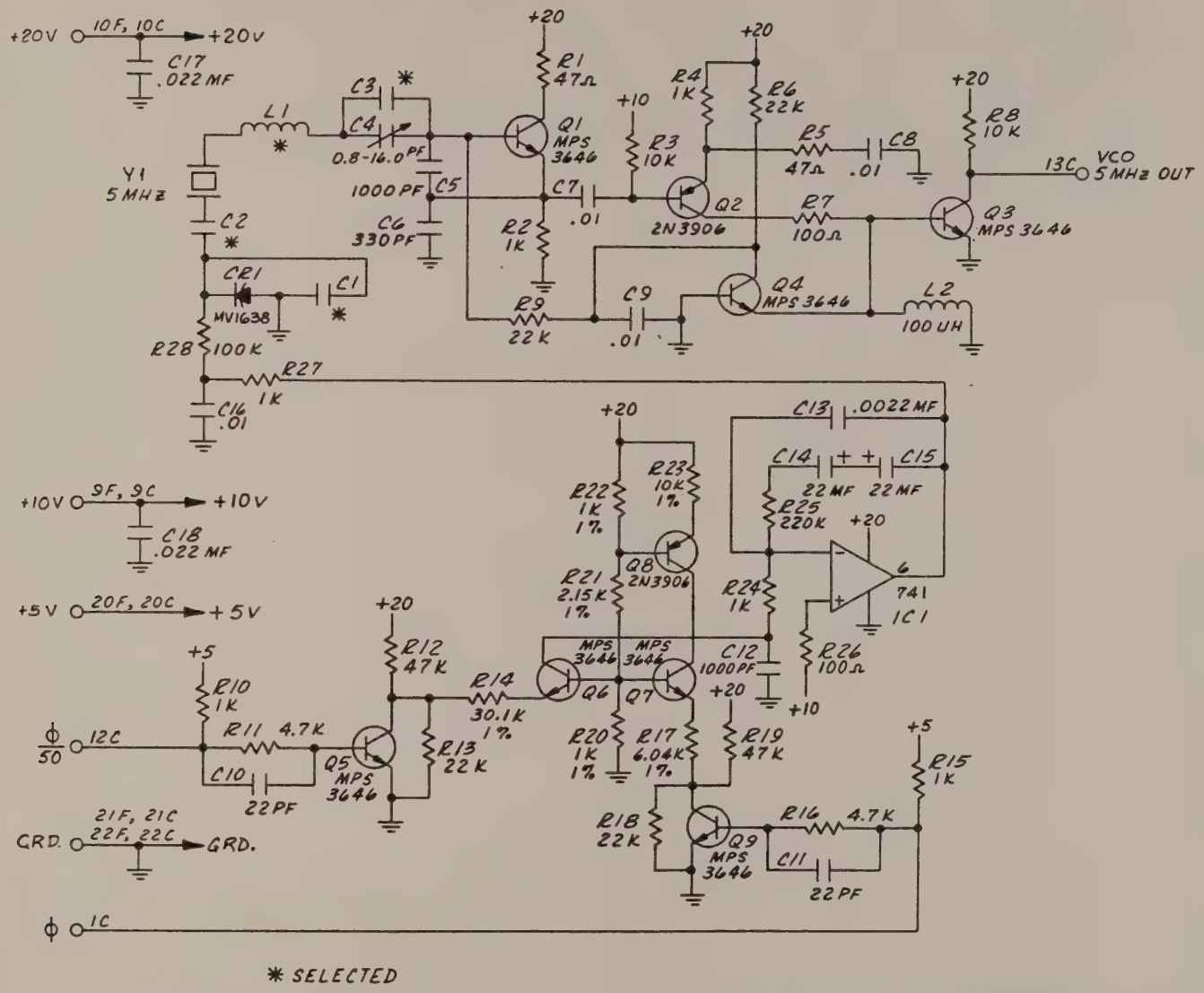
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | DUAL PHASE SHIFTER MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | | | SIZE 1 | CODE IDENT NO. 24672 | 10392172 REV B |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | | | |
| | | CHECK | CRL | 11-16-88 | | | |
| APPLICATION | | DRAWN | MLN | 11-88 | SCALE | | OF |

N O T E S :

4.3.10. 5 MHz VCO PCB A10
(Schematic Dwg. No. 12392286)

The 0 and 0/50 inputs at pins 1C and 12C are inverted and amplified by transistors Q5 and Q9, and summed in an amplifier formed by transistors Q6 and Q7 (Q8 provides a constant collector current for Q6 and Q7). The output of the amplifier is filtered by C12 and applied to the inverting input of operational amplifier (U1). The output of the operational amplifier is averaged by a low pass filter (R27 and C16) and applied across varicap CR1 to control the frequency of the 5 MHz oscillator. The maximum positive excursion of the waveform at the output of the oscillator (collector of Q3) is clamped at five volts by a diode (CR1) on PCB A13.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | |




FOR REFERENCE ONLY

| TOLERANCES UNLESS OTHERWISE SPECIFIED | | |
|---|---|---|
| DEC | FRAC | ANG |

MATERIAL:

| | | |
|---|---|---|
| Q.A. | | 18 Nov 88 |
| ENGR | CE | 17 Nov 88 |
| CHECK | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

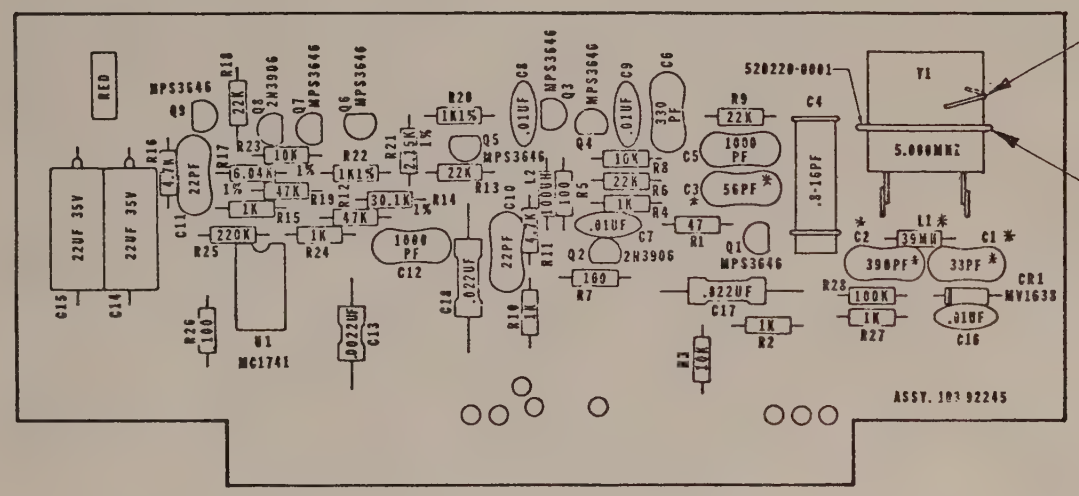
AUSTRON INC.
AUSTIN, TEXAS

5MHz VCO
MODEL 2010B

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 1 | 24672 | 12392286 | A |
| SCALE | | SHEET | OF |

| NEXT ASSY | USED ON |
|---|---|
| APPL | ON |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | D | ECO 1476; REDRAWN TO LATEST STD | 6/25/76 | RDB |
| | E | REVISED PARTS LIST PER ECO. 2823 | 4-16-79 | RDB |
| | F | REVISED P/L PER ECO 7978 88M | 10-21-85 | CL |
| | G | PL REVISED PER ECO 113807 | 1-13-88 | CAL |




SOLDER BUS WIRE ON CRYSTAL CASE SIDE OPPOSITE THE VACUUM EVACUATION PORT. #22 BUS- PUDDLE SOLDER TO CRYSTAL CASE

RUBBER STRAP

FOR REFERENCE ONLY

| QTY REQD | ITEM NO | REF DES | PART NO | NOMENCLATURE | VENDOR |
|---|---|---|---|---|---|
| -1 | | LIST OF MATERIAL | | | |

2. CIRCLED HOLES ARE FEED THROUGH HOLES
1. *INDICATES SELECTED VALUE, NOMINAL VALUES SHOWN

NOTES:

| | | | | |
|---|---|---|---|---|
| 2549214 7 | 2010 B | MATERIAL: | | |
| NEXT ASSY | USED ON | | | |
| APPLICATION | | | | |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DO NOT SCALE DRAWING

TOLERANCES UNLESS OTHERWISE SPECIFIED
DEC | FRACT | ANG

| | | |
|---|---|---|
| ENGINEER | | |
| CHECKED | RDB | 6-28-76 |
| DRAFTSMAN | KWIG | 6-25-76 |

AUSTRON INC AUSTIN TEXAS

PC BOARD ASSY, 5 MHZ VCO

| SIZE | CODE IDENT NO | | |
|---|---|---|---|
| 2 | 4-51 72 | 103 92245 | G |
| SCALE 1/1 | | SHEET 1 OF 1 | |

### 4.3.11. Digital Integrator PCB A11
### (Schematic Dwg. No. 12392283)

The 5 MHz output of the crystal oscillator is converted to a square wave by capacitor C1, resistors R3 and R4, and transistor Q1, then inverted by NOR gate (U4D). A differentiating circuit formed by transistor Q2 and IC (U2A) produces narrow negative pulses at the trailing edges of the square wave present at pin 10 of IC (U4D). These two signals are combined by NAND gates (U1A), (U1C) and (U1D) to produce 10 MHz outputs at pins 17C, 18C and 19C. R4 is adjusted to compensate for the delay in IC (U2B). The 1 MHz input at pin 8C is inverted by NOR gate (U4C) to produce a clock input to phase shifter A at pin 7C. The 1 MHz input at pin 8C is also divided by 100 by ICs (U5) and (U6) and gated with a 10 kHz signal (divided down from the 100 kHz input at pin 1F) to produce step and direction inputs to phase shifter B at pins 14C and 12C.

N O T E S :

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | A | 04E05 WERE MPS3704; R10 & R12 WERE 22K EC04291 | 6-24-83 | RJS |

P1-5C ← 5 MHz IN
R1 47.
R2 470
C1 .01
R3 2.2K
R4 5K
R5 1K
+5
Q1 MPS3646
7402 U4D
74H00 U2A
R7 680
R6 10K
* Q2 MPS3646
74H00 U1A
74H00 U1D
74H00 U1C
10 MHz OUT → P1-19C
10 MHz OUT → P1-18C
10 MHz OUT → P1-17C
74H00 2B
74H00 U1B
R8 10K
R9 680
* Q3 MPS3646
P1-20C, 20F ← +5
C3 .022
P1-21F, 21C, 22F, 22C ← GND → GND
1 MHz TO Ø SHIFT A → P1-7C
Ø/50 → P1-15C
P1-8C ← 1MHz
7402 U4C
P1-1F ← 100 KC FROM Ø SHIFT A
U7 7490 ÷10
U6 7490 ÷10
U5 7490 ÷10
74H00 U2D
R10 10K
R11 4.7K
Q4 MPS3646
U3A 7474 CLOCK CLEAR
7402 U4B
R16 4.7K
MPS3646 Q7
C2 1
R17 4.7K
DIRECTION (Ø SHIFT B) → P1-12C
7402 U4A
U3B 7474 CLOCK CLEAR
STEP (Ø SHIFT B) → P1-14C
74H00 U2C
R12 10K
R13 4.7K
Q5 MPS3646
R15 4.7K
Q6 MPS3646
R14 4.7K

*SELECTED PAIR IN TEST
≤ 60 NSEC RISE TIME
≤ 10 NSEC RISE TIME DIFFERENCE

FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO |
|---|---|---|---|
| | 2010B | A11 | |

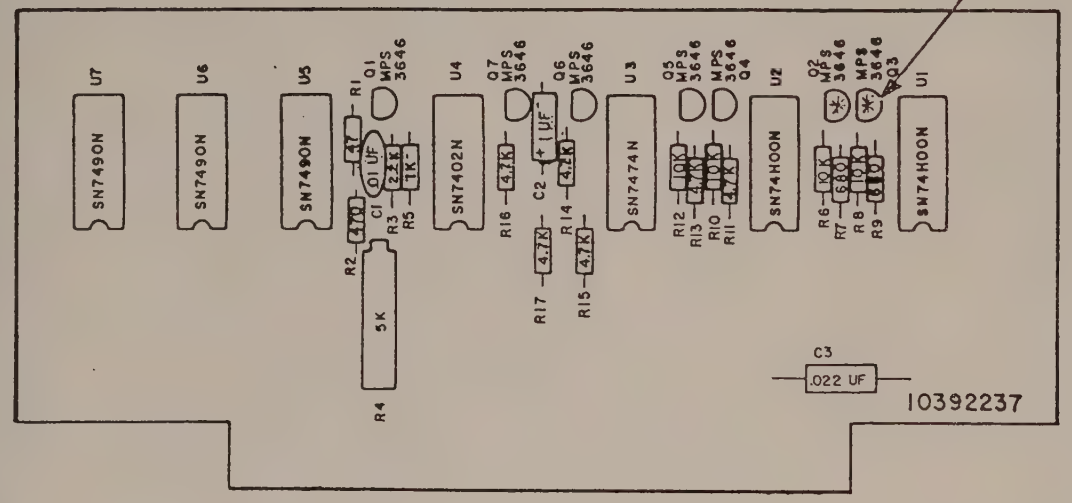
TOLERANCES UNLESS OTHERWISE SPECIFIED: DECIMALS | FRACTIONS | ANGLES
MATERIAL:
ENGR 6-28-83
CHECKED 6-28-83

AUSTRON INC. AUSTIN, TEXAS

SCHEMATIC – DIGITAL INTE – GRATOR MODEL 2010B

SIZE 4 | 4-55 | 12392283 | A

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| 3C | C | Q4&Q5 WERE MPS3704; R10&R12 WERE 22K ECO 4281 | 8-8-83 | RJS |




FOR REFERENCE ONLY

*1. SELECTED PAIR IN TEST
≧60 NSEC RISE TIME
≧10 NSEC RISE TIME DIFFERENCE

NOTES:

| NEXT ASSY | USED ON | REF DES | FIG NO. |
|---|---|---|---|
| 12392283 | 2010 B | | |

APPLICATION

TOLERANCES UNLESS OTHERWISE SPECIFIED

| DEC | FRAC | ANG |
|---|---|---|
| | | |

MATERIAL:

| | | |
|---|---|---|
| ENGR | | |
| CHECK | [illegible] | 8-8-83 |
| DRAWN | SHAW | 8583 |

AUSTRON INC.
AUSTIN, TEXAS

PCB ASSY, DIGITAL INTEGRATOR.

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 2 | 4-57 | 10392237 | C |

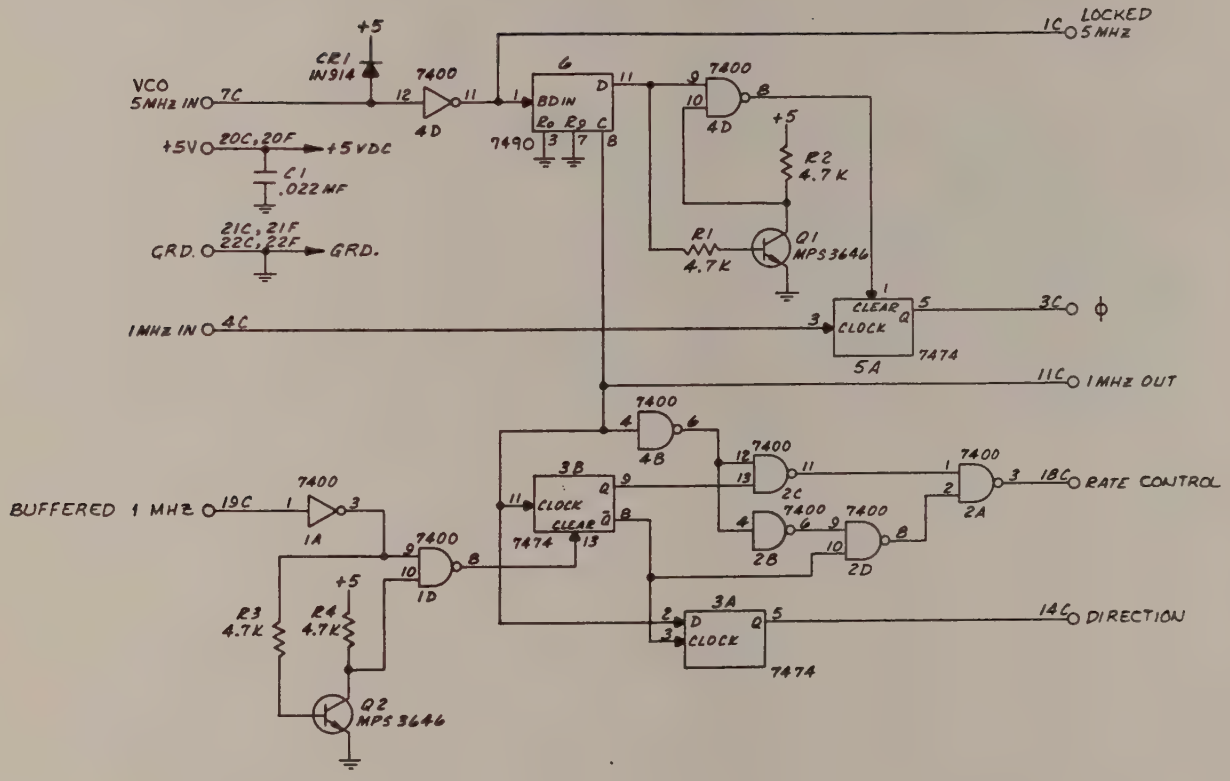
SCALE 1/1 SHEET 1 OF 1

### 4.3.12. Phase Detector PCB A13 (Schematic Dwg. No. 12392285)

Diode CR1 clamps the positive excursion of the input at pin 7C (coming from the collector of Q3 on A10) to 5 Vdc. This converts the output of the 5 MHz VCO to a logic level suitable for driving series SN7400N-type integrated circuits. IC (U4C) inverts the input and provides a 5 MHz output at pin 1C. IC (U6) is an SN7490N connected as an N/5 divider, producing 1 MHz outputs at pins 8 and 11. The 1 MHz output at pin 11 of IC (U6) is applied to a transistor-integrated circuit differentiator Q1 and IC (U4D) which produces narrow negative-going pulses at pin 8. The 1 MHz output of NAND gate (U4D) is applied to the clear input of IC (U5A), a D-type flip-flop (SN7474N). A 1 MHz input at pin 4C drives the clock input of IC (U5A).

This arrangement produces a 1 MHz variable duty cycle square wave output at pin 3C. The duty cycle of the square wave is proportional to the relative phase difference between the clock and clear inputs to IC (U5A). If the clear input advances in phase with respect to the clock input, the positive duty cycle of the output will decrease. The buffered 1 MHz reference input at pin 19C is inverted by IC (U1A) and applied to the input of a transistor-integrated circuit differentiator composed of Q2 and IC (U1D). The negative-going pulses at the output of NAND gate (U1D) are gated with the 1 MHz output at pin 18C (used to control the rate of the unijunction oscillator on A14) and a direction output for a variable ratio divider at pin 14C.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| A | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| TOLERANCES UNLESS OTHERWISE SPECIFIED | | |
|---|---|---|
| DEC | FRAC | ANG |
| MATERIAL: | | |

AUSTRON INC.
AUSTIN, TEXAS

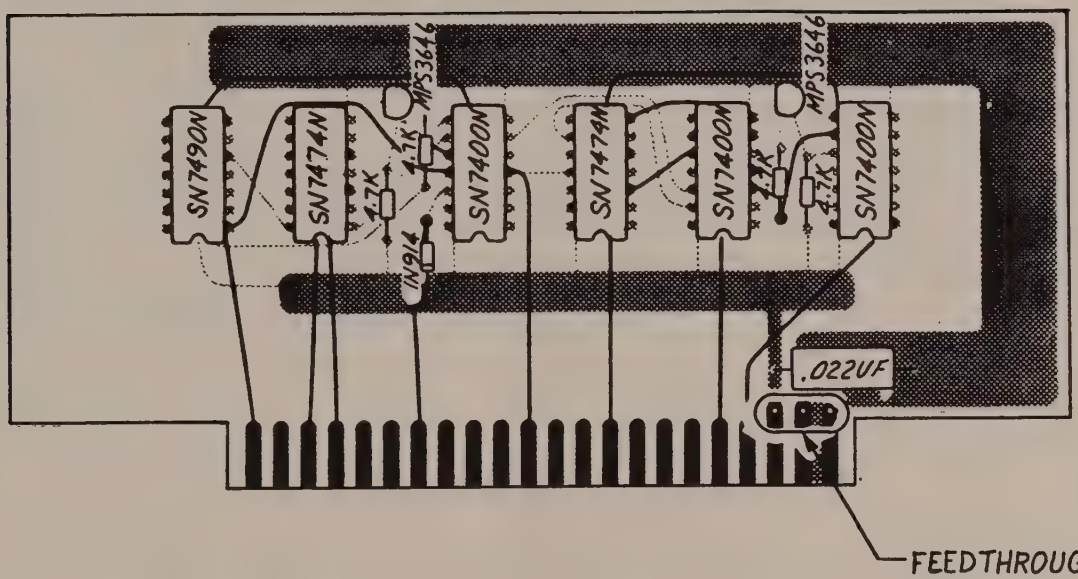
**PHASE DETECTOR**
**MODEL 2010B**

| | | |
|---|---|---|
| Q.A. | | 18 Nov 88 |
| ENGR | CE | 17 Nov 88 |
| CHECK | CRL | 11-16-88 |
| DRAWN | MLN | 11-88 |

| SIZE | CODE IDENT NO. | | REV |
|---|---|---|---|
| 1 | 24672 | 12392285 | A |
| SCALE | | SHEET | OF |

| NEXT ASSY | USED ON |
|---|---|
| APPLI 4-60 | N |

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




FOR REFERENCE ONLY

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | | |
| | | DEC | FRAC | ANG | PHASE DETECTOR MODEL 2010B | | | |
| | | MATERIAL: | | | | | | |
| | | Q.A. | | 8 Nov 88 | SIZE | CODE IDENT NO. | | REV |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | 1 | 24672 | 10392219 | B |
| APPLICATION | | CHECK | CRL | 11-16-88 | | | | |
| | | DRAWN | MLN | 11-88 | SCALE | | SHEET 4-61 OF | |

N O T E S :

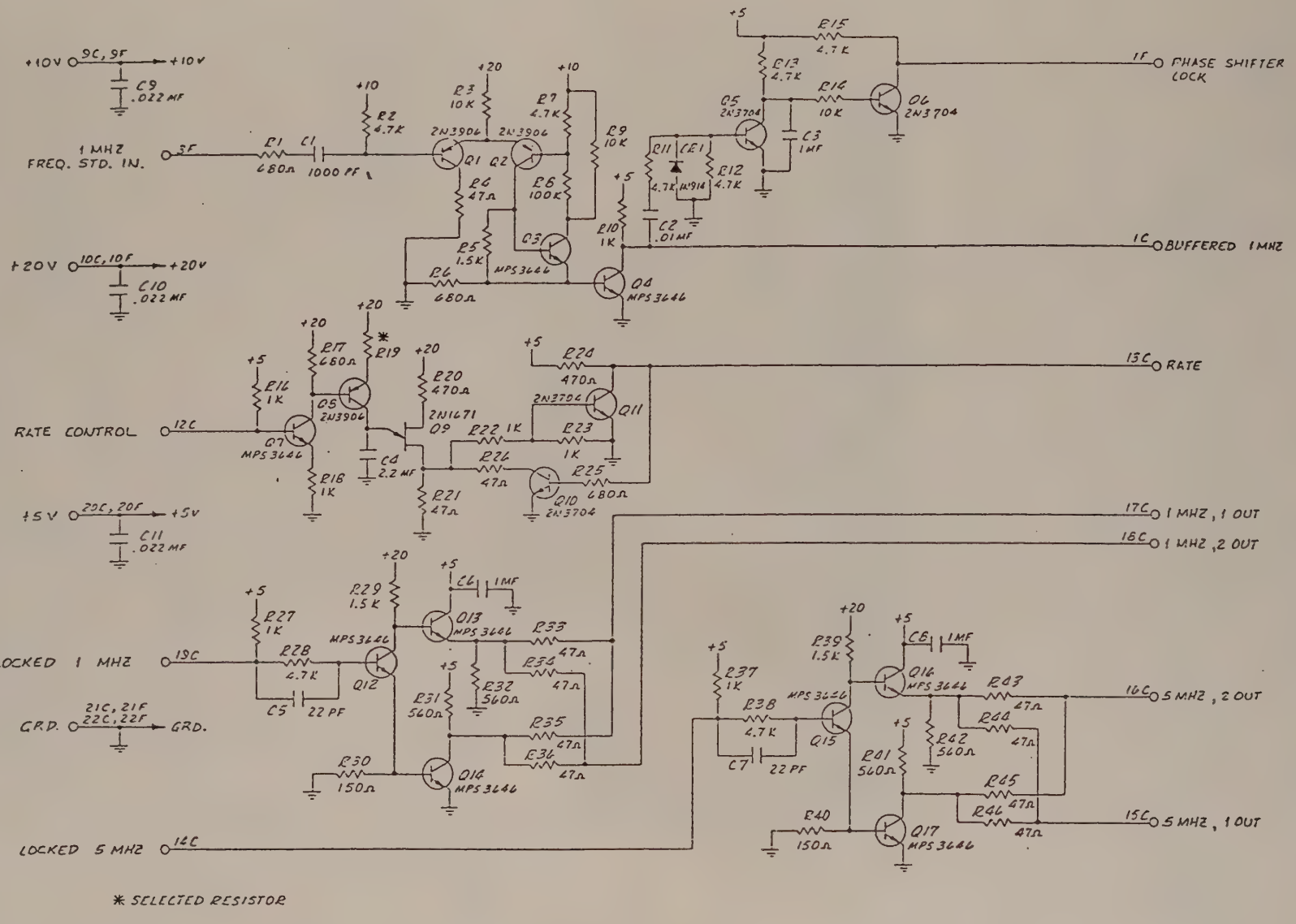
### 4.3.13. Input/Output Buffers PCB A14 (Schematic Dwg. No. 12392289)

The circuits on PCB A14 contain an input buffer and detector, a unijunction oscillator, and two output buffers. Transistors Q1, Q2, Q3 and Q4 amplify and square the 1 MHz frequency standard input, producing a 5 Vp-p output at pin 1C. As long as the 1 MHz frequency standard input to the unit is present, C2, R11, R12 and CR1 differentiate the square wave at the collector of Q4, producing positive spikes at a 1 MHz rate at the base of Q5 to keep Q5 turned on and C3 discharged. When the 1 MHz frequency standard input is absent, C3 is allowed to charge through R13 toward the positive 5 volts supply, turning Q6 on. The output at pin 1F will be a logic ONE (5 volts) when the frequency standard input is present and a logic ZERO (zero volts) when the frequency standard input is absent.

Transistor Q8 acts as a variable resistance in the charge path of C4. A variable duty cycle 1 MHz square wave at the base of Q7 controls the length of time Q8 is turned on and thus the output frequency of the unijunction Q9. Transistors Q11 and Q10 amplify and square the output pulses produced at pin 13C. Transistors Q12, Q13 and Q14 form a buffer amplifier designed to produce a 1 MHz square wave output at a constant 50 ohm impedance. Transistors Q15, Q16 and Q17 form a similar buffer for the 5 MHz rear panel outputs.

N O T E S :

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPD |
| | | | 8-19 FS | |




FOR REFERENCE ONLY

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| | | | | |
| | | | | |
| | 2010B | A14 | | |
| NEXT ASSY | USED ON | REF DES | FIG NO | |
| APPLICATION | | | | |

TOLERANCES UNLESS OTHERWISE SPECIFIED

| DECIMALS | FRACTIONS | ANGLES |
|---|---|---|
| | | |

MATERIAL:

ENGR

CHECKED

DRAWN [illegible] 8.10.65

AUSTRON INC.
AUSTIN, TEXAS

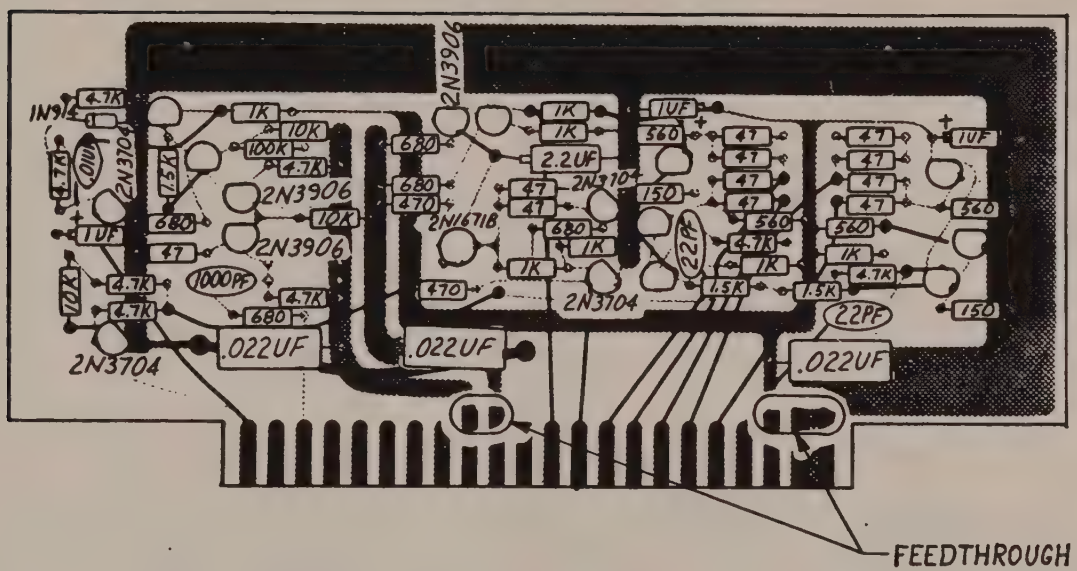
# SCHEM, INPUT/OUTPUT BUFFERS MODEL 2010B-A14

| SIZE | | | |
|---|---|---|---|
| 3 | 4-65 | 12392289 | — |

SCALE NONE

SHEET 1 OF 1

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| B | REDRAWN PER ECO 12060 MLN | 11/18/88 | CRL |




2. TRANSISTORS ARE MPS3646
1. RESISTANCE VALUES ARE IN OHMS
NOTES: UNLESS OTHERWISE SPECIFIED

FOR REFERENCE ONLY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | | | |
| | | MATERIAL: | | | INPUT / OUTPUT BUFFERS MODEL 2010B | | |
| | | Q.A. | Joe L | 18 Nov 88 | SIZE | CODE IDENT NO. | REV |
| NEXT ASSY | USED ON | ENGR | CE | 17 Nov 88 | 1 | 24672 | 10392243 B |
| APPLICATION | | CHECK | CRL | 11-16-88 | | | |
| | | DRAWN | MLN | 11-88 | SCALE | | T OF |

NOTES:

# 5. MAINTENANCE

## 5.1. SCOPE OF SECTION

Section Five describes the procedure for calibrating the Model 2010B Disciplined Frequency Standard and suggests a general approach for troubleshooting the unit.

The Model 2010B Disciplined Frequency Standard PCBs are mounted in the Interconnect PCB in the following order:

| | |
|---|---|
| A1 | 20 Volt and 5 Volt Regulator |
| A2 | 10 Volt Regulator |
| A2 | Differentiator |
| A4 | Phase Comparator |
| A5 | Divider 1 |
| A6 | Divider 2 |
| A7 | Divider 3 |
| A8 | Servo Control |
| A9 | Dual Phase Shifter |
| A10 | 5 MHz VCO |
| A11 | Digital Integrator |
| A12 | Dual Phase Shifter |
| A13 | Phase Detector |
| A14 | Input/Output Buffers |

## 5.2. PRINTED CIRCUIT BOARD PIN NUMBERING SYSTEM

The side of a PCB on which the electrical components are mounted has been designated the component side of the board. The pins have been assigned numbers from 1 to 22 beginning at the edge nearer the front panel and ending at the edge nearer the rear panel. For example, the third pin from the front edge on the component side of the DIVIDER 1 PCB would be referred to as pin A5-3C and it would mate with XA5-3C in the Interconnect board connector.

The opposite side of the board (on which most, although not necessarily all, of the interconnections between components are made) has been designated the foil side. The pin on the foil side are also numbered from 1 to 22 beginning at the edge near the front panel and ending at the edge nearer the rear panel.

## 5.3. TROUBLESHOOTING

Using the schematics and assembly drawings of the PCBs in Section Four, the standard procedure for finding a malfunction is to trace back from the obvious loss of output until the trouble is located. Of course, where a total loss of outputs occurs, the power supply voltage should be checked first.

## 5.4. CALIBRATION

The following are step-by-step procedures for calibrating the 2010B Disciplined Frequency Standard. To locate the components described in the following tables, refer to the assembly drawings of the PCB concerned.

Adjustment requires removal of the top cover from the chassis.

Table 5-1: Calibrating The 20 Volt and 5 Volt Regulator PCB A1

| STEP | PROCEDURE |
|---|---|
| 1 | Set ac switch to OFF |
| 2 | Remove top cover |
| 3 | Set ac switch to ON |
| 4 | Connect negative voltmeter lead to ground (pins 21 and 22) and positive lead to 5 volts output (pin 20) |
| 5 | Adjust R18 for voltmeter reading of 4.9 ±0.1 volts |

Adjustment requires removal of the top cover from the chassis.

Table 5-2: Calibrating The 5 MHz VCO PCB A10

| STEP | PROCEDURE |
|---|---|
| 1 | Set ac switch to OFF |
| 2 | Remove top cover |
| 3 | Remove A10 from chassis and mount on an Extender PCB |
| 4 | Set ac switch to ON |
| *5 | Wait two hours for 5 MHz crystal oscillator to stabilize |

CALIBRATION (continued)

| STEP | PROCEDURE |
|---|---|
| 6 | Connect oscilloscope X10 attenuator probe to pin 1C of A10 and verify that signal at this point has a 40 to 60% duty cycle |
| 7 | Connect scope probe to pin 6 of IC (U1) on A10 and adjust C4 until voltage at pin 6 is 8 volts |

NOTE

If the crystal oscillator has been on for longer than two hours, this step can be omitted if the power switch is placed in the OFF position only as long as required to place the PCB on an extender.

Adjustment requires removal of the top cover.

Table 5-3: Calibrating The Digital Integrator PCB A11

| STEP | PROCEDURE |
|---|---|
| 1 | Set ac switch to OFF |
| 2 | Remove top cover |
| 3 | Set ac switch to ON |
| *4 | Wait two hours for 5 MHz crystal oscillator to stabilize |
| 5 | Connect oscilloscope X10 attenuator probe to pin 17C of A11 and verify that 10 MHz positive-going pulses are present |
| 6 | Repeat Step 5 at pins 18C and 19C |
| 7 | Reconnect scope probe to pin 17C and adjust R4 until spacing between pulses is equal |

NOTE

If the crystal oscillator has been on for longer than two hours, this step can be omitted if the power switch is placed in the OFF position only as long as required to place the PCB on an extender.

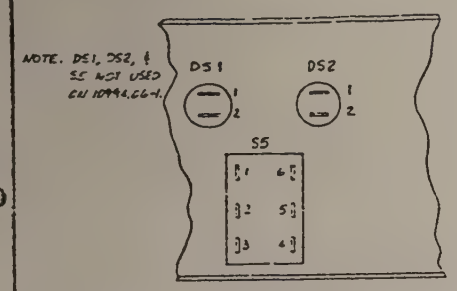
Adjustment requires removal of the top cover.

Table 5-4: Calibrating The Phase Comparator PCB A4

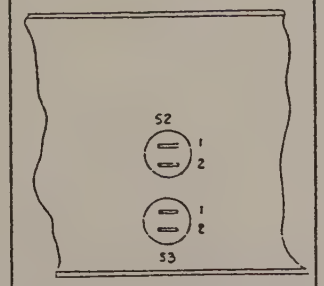
| STEP | PROCEDURE |
|---|---|
| 1 | Set ac switch to OFF |
| 2 | Remove top cover |
| 3 | Set ac switch to ON |
| 4 | Set front panel CONTROL Mode switch to SET CONTROL position |
| 5 | Set to AGING position |
| 6 | Press INCREASE push button until indicator on front panel meter reaches maximum positive reading and recycles |
| 7 | Adjust R25 on A4 until recycle point occurs at 5 on meter scale. |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APP'D |
| | F | REDRAWN AND CREATED -1 PER ECO 2346 | 2-3-83 | |
| | G | ADDED NO. LOCK WASHERS ECO 7854 | 10-3-85 | |

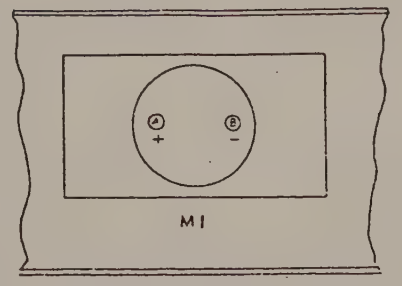
NOTE. DS1, DS2, & S5 NOT USED ON 10994106-1.



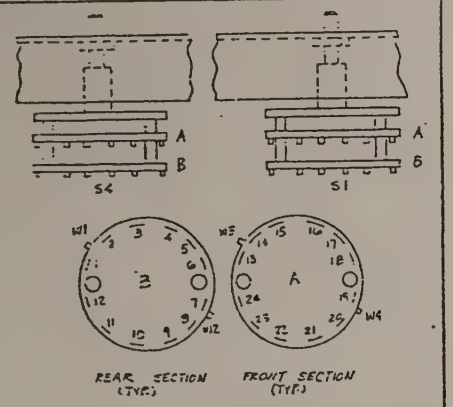

REAR VIEW of DETAILS DS1, DS2, & S5



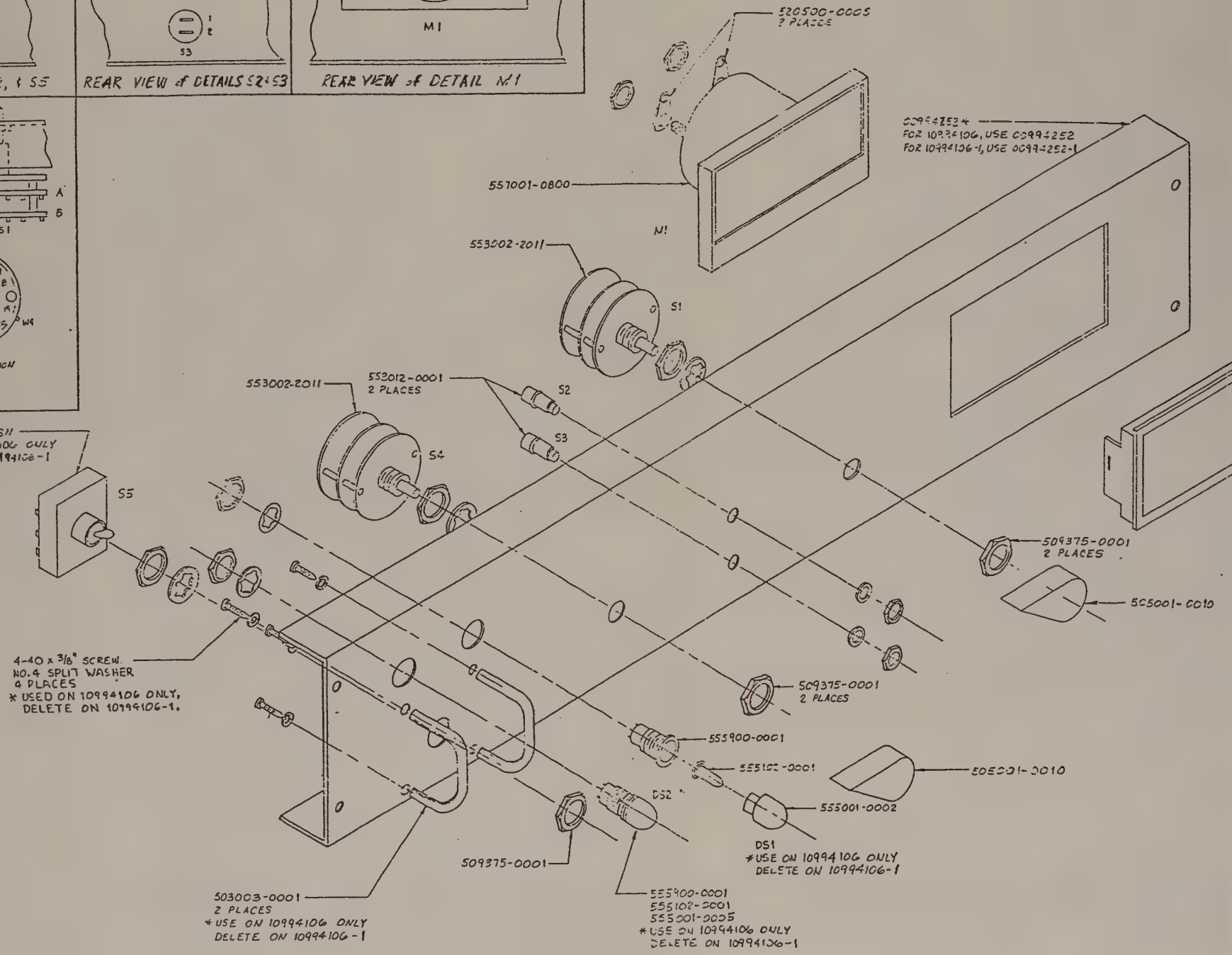

REAR VIEW of DETAILS S2 & S3




REAR VIEW of DETAIL M1




DETAILS S1 & S4




FOR REFERENCE ONLY

| NEXT ASSY | USED ON | REF DES | FIG NO |
|---|---|---|---|
| 20496710-1 | 2010K | | |
| 20496710 | 2010B | | |

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMALS | FRACTIONS | ANGLES

MATERIAL:

ENGR Jim Porter 2-3-83
CHECKED 2-3-83

AUSTRON INC. AUSTIN, TEXAS

PANEL ASS'Y, INNER FRONT

SIZE 4 | 5-5 | 10994106 * | G

# ERRATA SHEET
Model 2010B
Disciplined Frequency Standard
P/N 12794207, Revision C
June 19, 1995

This errata sheet reflects minor changes to the Model 2010B Manual per Engineering Change Order Numbers as listed:

| ECO | Effective Date |
|---|---|
| 12228 | January 4, 1989 |

1. To Assembly Dwg. No. 10392245, revision G, page 4-51. No change to drawing except for new revision level of H.

| ECO | Effective Date | Serial Numbers Effected |
|---|---|---|
| 12418 | March 28, 1989 | S/N 10304W and subsequent |

1. To Inner Front Panel Assy, Dwg. No. 10994106-*, revision G, page 6-3.
   a. In zone C5 change P/N 557001-0800 to 557001-0820, change P/N 520500-0005 to 520503-0000, change P/N 555001-0002 to 555500-0002, change P/N 555001-0005 to 555500-0005.
   b. In zone B7 add to No. 4 split lock wshr: 400152-0000
   c. In zone B7 add to 4-40 x 3/8" screw PNH PHH: P/N 400040-0015.
   d. In zone B4 remove 2 ea. split lock washers shown to install P/N 553012-0001.
   New revision of Dwg. No. 10994106-* is H.

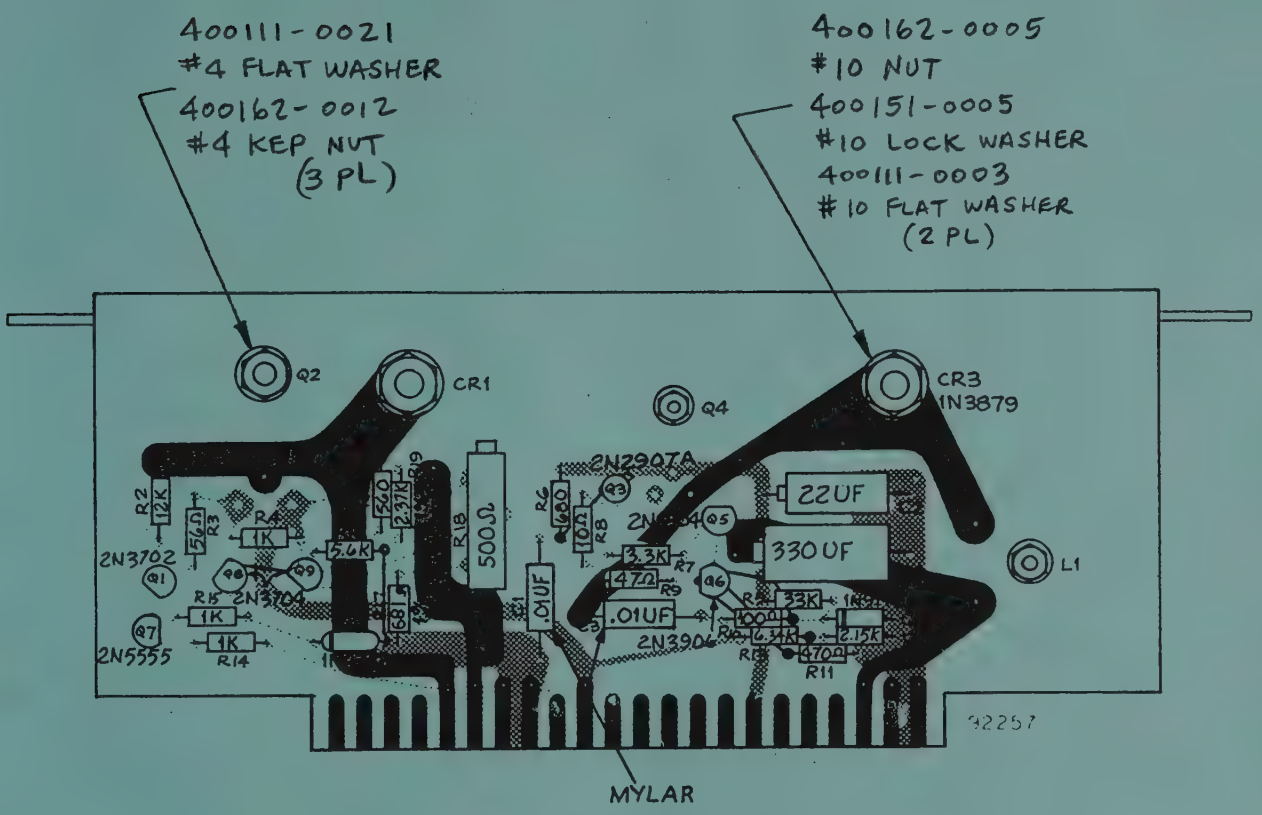
| ECO | Effective Date | Serial Numbers Effected |
|---|---|---|
| 12507 | April 26, 1989 | S/N 10304W and subsequent |

1. To Inner Front Panel Assy, Dwg. No. 10994106-*, revision G, page 6-3. In zone A5, change P/N 555501-0005 to P/N 555500-0005.
   New revision of Dwg. No. 10994106-* is J.

| ECO | Effective Date | Serial Numbers Effected |
|---|---|---|
| 12809 | October 19, 1989 | S/N 10941X and subsequent |

1. To assembly Dwg. No. 10392258, revision H, page 4-9.
   a. Show location of new hardware.
   b. Add NOTE 1 to drawing.
   See attached drawing for changes.
   New revision of Dwg. No. 103922258 is now J.

| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE | APPD |
| H | REDRAWN PER ECO 12060 MLN | 11/16/88 | CRL |
| J | REV PER ECO 12809 MLN | 10/31/89 | |




## ( COMPONENT SIDE )

FOR REFERENCE ONLY

NOTES:

1. INSTALL INSULATOR (510903-1002) IN HEATSINK (00492217) THEN INSTALL CR1 & CR3.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | TOLERANCES UNLESS OTHERWISE SPECIFIED | | | AUSTRON INC. AUSTIN, TEXAS | | |
| | | DEC | FRAC | ANG | +20 +5 V REGULATOR MODEL 2010B | | |
| | | MATERIAL: | | | | | |
| | | Q.A. | Joe | 12/Nov/88 | SIZE 1 | CODE IDENT NO. 24672 | 10392258 REV J |
| NEXT ASSY | USED ON | ENGR | CE | 12/Nov/88 | | | |
| APPLICATION | | CHECK | CRL | 11-16-88 | SCALE | | SHEET 1 OF 2 |
| | | DRAWN | MLN | 11-88 | | | |

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